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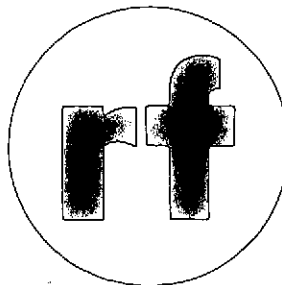
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RF COMMUNICATIONS, INC.



FINAL
DESIGN EVALUATION REPORT
S-BAND EXCITERS
CONTRACT NO. NAS5-20464

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TABLE OF CONTENTS

<u>Section</u>	<u>Title</u>	<u>Page</u>
1.0	INTRODUCTION.	1-1
2.0	PERFORMANCE OBJECTIVES.	2-1
2.1	General Objectives.	2-2
2.2	Detailed Performance Requirements . . .	2-2
3.0	SYSTEM DESIGN	3-1
3.1	General	3-1
3.1.1	Electrical Building Blocks.	3-4
3.2	Exciter Subsystem	3-7
3.2.1	Synthesizer	3-10
3.2.1.1	Synthesizer VCO Module.	3-14
3.2.1.2	Programmable Divider/Phase Detector . .	3-16
3.2.1.3	Fine Loop Translator Module	3-24
3.2.1.4	Intermediate Loop Translator Module . .	3-26
3.2.2	Reference Frequency Generation.	3-28
3.2.2.1	Frequency Standard.	3-31
3.2.2.2	250 kHz/13.5 MHz Generator.	3-32
3.2.2.3	40/175/190 MHz Generator.	3-34
3.2.2.4	75/150/265 MHz Generator.	3-36
3.2.3	Search VCXO Module.	3-38
3.2.4	VCXO Multiplier/Phase Detector.	3-40
3.2.5	Loop Filter/Acquisition Circuits. . . .	3-43
3.2.6	Up Converter.	3-51
3.2.7	FM Generator.	3-54
3.2.8	Phase Modulator/Modulation Input Circuits	3-59
3.2.9	$f_T/32$ Doppler Output.	3-64
3.2.10	$19f_T/221$ Generator.	3-67
3.3	Verification Receiver	3-71
3.3.1	L.O. Translator	3-73
3.3.2	IF Amplifier.	3-75
3.3.3	FM Demodulator.	3-77
3.3.4	PM Demodulator.	3-79
3.3.5	Phase Shift Keyed Demodulator	3-81
3.4	Exciter Controls and Monitors	3-83
3.4.1	Local Exciter Control	3-84
3.4.2	Test Controls	3-91
3.4.2.1	Local Exciter Test Control Panel. . . .	3-92
3.4.2.2	Antenna Control	3-94
3.5	Remote Control Panel.	3-97
3.6	System Interface.	3-98a
3.7	Exciter Subsystem Mechanical Design . .	3-99
3.7.1	Exciter Rack Layout	3-104
3.8	Antenna Equipment	3-106
3.8.1	Antenna Electronics	3-107
3.8.1.1	Times Four Multipliers.	3-110
3.8.1.2	S-Band Amplifier.	3-112
3.8.1.3	Verification Receiver Down Converter. .	3-120
3.8.2	Output Combiner	3-122
3.8.3	Frequency Translator.	3-124

TABLE OF CONTENTS
(Cont.)

<u>Section</u>	<u>Title</u>	<u>Page</u>
3.8.4	Antenna Equipment Mechanical Design . .	3-127
3.8.5	Thermal Analysis.	3-130
4.0	SYSTEM ANALYSIS	4-1
4.1	Phase Noise	4-1
4.1.1	Analysis of the Requirement	4-1
4.1.2	Phase Noise Model of the Exciter. . . .	4-3
4.2	Spurious Response	4-11
4.3	Time Delay Analysis	4-15
4.4	Exciter VCXO Offset Decay	4-17
5.0	SYSTEM TESTING.	5-1
5.1	General	5-1
5.2	S-Band Exciter Acceptance Tests	5-2

APPENDIX I

5 MHz Frequency Standard Specification

APPENDIX II

An MTBF Calculation and
Percent Operability Prediction

APPENDIX III

Cable Assemblies

Operations Building to Antenna
Frequency Translator to Antenna Control

LIST OF ILLUSTRATIONS

<u>Figure</u>	<u>Title</u>	<u>Page</u>
3.1.1	S-Band Exciter System Physical Configuration.	3-2
3.2.1	S-Band Exciter Frequency Synthesizer Diagram.	3-8
3.2.2	Frequency Synthesizer	3-11
3.2.3	Synthesizer VCO Module.	3-15
3.2.4	Divide by "N" Module.	3-17
3.2.5	Programmable Divider Block Diagram. . .	3-19
3.2.6	Phase Detector/Coarse Tune Generator. .	3-21
3.2.7	Fine Loop Translator.	3-25
3.2.8	Intermediate Loop Translator.	3-27
3.2.10	Reference Generator - 250 kHz/13,5 MHz. .	3-33
3.2.11	40/175/190 MHz Generator.	3-35
3.2.12	75/150/265 MHz Generator.	3-37
3.2.13	Search VCXO Module.	3-39
3.2.14	Search VCXO Multiplier/Phase Detector .	3-41
3.2.15A	Loop Filter/Acquisition Circuits. . . .	3-44
3.2.15B	Correlation Detector.	3-45
3.2.16	Up Converter.	3-52
3.2.17	FM Generator.	3-55
3.2.18	Phase Modulator	3-60
3.2.19	$f_T/32$ Doppler Output.	3-65
3.2.20	$19f_T/221$ Generator.	3-68
3.3.1	Verification Receiver Block Diagram . .	3-72
3.3.2	L.O. Translator	3-74
3.3.3	FM Demodulator.	3-78
3.3.4	PM Demodulator.	3-80
3.3.5	PSK Demodulator	3-82A
3.4.1	Exciter Control Panel	3-85
3.4.2	Control Interface Logic	3-88
3.4.3	Exciter Control Drawer Block Diagram. .	3-89
3.4.4	Local Control Panel	3-92
3.4.5	Antenna Control Panel	3-94
3.4.6	Test/Antenna Control.	3-96
3.5.1	Remote Control Panel.	3-98
3.6.1	System Interface.	3-98b
3.6.2	Control Cables.	3-98c
3.6.3	RF Interconnecting Cables	3-98d
3.7.1	Typical Drawer Layout	3-100
3.7.2	Module Construction	3-101
3.7.3	Demodulator Module Installation	3-103
3.7.4	Exciter Rack Layout	3-105
3.8.1	Antenna Electronics	3-108
3.8.2	Automatic Power Control	3-109
3.8.3	4X Frequency Multiplier	3-111
3.8.4	S-Band Driver Amplifier	3-115
3.8.5	24 Watt Power Amplifier	3-118

LIST OF ILLUSTRATIONS
(Cont.)

<u>Figure</u>	<u>Title</u>	<u>Page</u>
3.8.6	Verification Receiver Down Converter. .	3-121
3.8.7	Combiner.	3-123
3.8.8	Translator.	3-125
3.8.9	Frequency Translator Mechanical Design.	3-126
3.8.10	Antenna S-Band Amplifier Layout	3-129
4.1.1	S-Band Exciter Phase Noise Model. . . .	4-4
4.1.2	MFR Synthesizer Phase Noise One-Sided Power Density.	4-5
4.1.3	Phase Noise Test Set-Up	4-6
4.1.4	300 MHz Phase Noise Power One-Sided Power Density.	4-8
4.3.1	Exciter Time Delay Distribution	4-16
4.4.1	Decay Voltage Integration Diagram . . .	4-18
4.4.2	Integrator Waveforms.	4-19
5.2.1	Phase Noise Test Set-Up	5-3
5.2.2	FM Distortion Test Set-Up	5-5
5.2.3	PM Distortion Test Set-Up	5-6

1.0 INTRODUCTION

This report contains the results of a design evaluation study conducted as a part of a contract to produce S-Band Exciter (SBE) systems for the Goddard Space Flight Center. The work was performed by the Government Products Division of RF Communications Division, Harris-Intertype Corporation, under Contract No. NAS5-20464 dated 3 DEC 73.

The purpose of the report is to define the performance objectives of the SBE and to describe in detail a design which will meet these objectives.

2.0 PERFORMANCE REQUIREMENTS

2.1 General Objectives

The S-Band Exciter (SBE) is required to provide a highly stable phase or frequency modulated carrier for transmission to spacecraft. The exciter will be used as part of an S-Band Receiver/Exciter/Ranging system at Spaceflight Tracking and Data Network (STDN) ground stations. Major features in the design include:

- a) Synthesized S-Band, 2025 to 2120 MHz, signal tunable in 100 Hz increments.
- b) Search VCXO with selectable ± 15 kHz or ± 300 kHz search range.
- c) Phase modulated, frequency modulated, or phase-shift-keyed carrier.
- d) Solid state 16 watt S-Band Amplifier.
- e) 240/221 Coherent Frequency Translator to provide the 2200 - 2300 MHz receive frequency for system testing.
- f) Verification Receiver, coherently tuned to exciter output frequency, with PM, FM, or PSK demodulators.
- g) Provision for local control, remote control with local set-up, or remote control with computer set-up.
- h) Test Mode with provision for sweeping the PA.
- i) Generates an unmodulated signal at $1/32$ of the output frequency as a reference to the ranging equipment.
- j) Modular construction to facilitate maintenance.

2.2 Detailed Performance Requirements

The S-Band Exciter (SBE) performance requirements are dictated by GSFC Specification 73-15078 REVISED November, 1973, and clarifications thereof as defined in Design Review Minutes, March 1974.

3.0 SYSTEM DESIGN

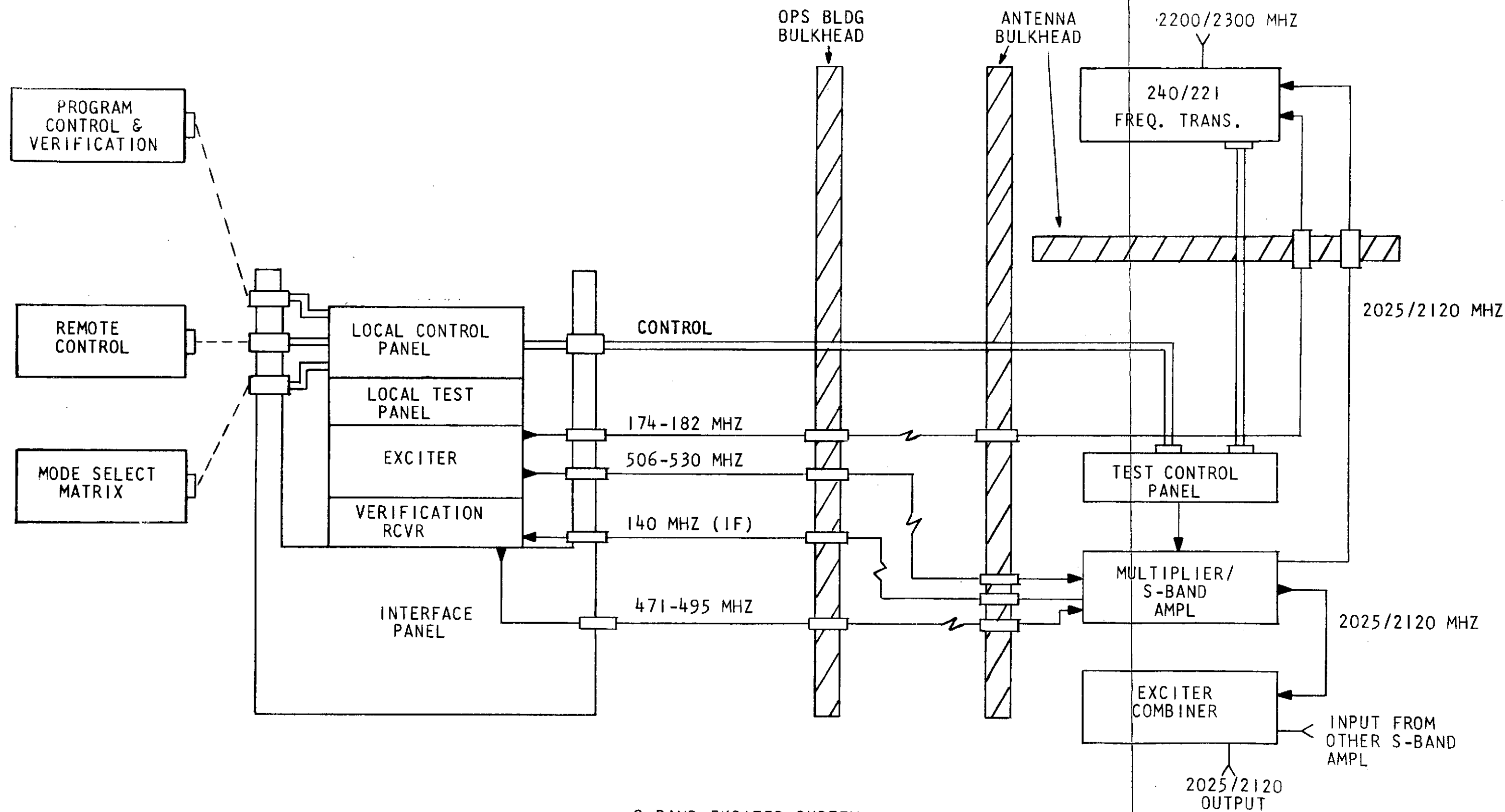
3.1 General

The S-Band Exciter system is divided into two major subsystems: (1) Operations Control Building Equipment and (2) Antenna Equipment. The physical configuration of the exciter system is illustrated in Figure 3.1.1.

The Operations Control Building Equipment comprises the following units:

- a) Exciter Drawer - Synthesizes the 2025 to 2125 MHz carrier from an internal 5 MHz frequency standard or an external 1 or 5 MHz standard. Provides for PM, FM or PSK modulating the carrier. Also includes the search VCXO and acquisition circuits. Coherent unmodulated signals are provided for the verification receiver local oscillator, the frequency translator and the doppler extractor reference.
- b) Verification Receiver - Processes the down converted exciter or PA output signal to provide PM, FM and PSK demodulated video outputs.
- c) Exciter Control - Provides control signals to the exciter drawer and acts as a Computer/Remote Control interface. Contains the regulated power supplies for the rack mounted equipment.
- d) Exciter Test Control - Provides control to the frequency translator and sweep voltage to the exciter.

These units, along with a second exciter, are housed in a



S-BAND EXCITER SYSTEM
PHYSICAL CONFIGURATION

FIGURE 3.1.1

FOLDOUT FRAME

FOLDOUT FRAME

standard equipment rack. In addition, the Operations Control Building Equipment includes a Remote Control unit which is used with the Computer or Local Exciter Control unit to operate the exciter.

The Antenna Equipment comprises the following units:

- a) S-Band Amplifier - This unit accepts the 506.25 to 530 MHz output from the exciter drawer in the Operations Control Building, multiplies it to 2025 to 2120 MHz and provides 16 watts to the power amplifier. The verification receiver down converter is also located in this unit and an IF signal is sent back to the Operations Control Building.
- b) Frequency Translator - Accepts signals from the exciter ($19 f_T/221$) and the S-Band amplifier (f_T) to provide an output at 2200 to 2300 MHz ($240/221 f_T$) for testing the system.
- c) Output Combiner - Provides means to combine the outputs of two exciters (at different frequencies) into one output. Also provides for bypassing the power amplifier.
- d) Antenna Control Panel - Provides for control and testing of the S-Band amplifier/power amplifier from the antenna location.

3.1.1 Electrical Building Blocks

Throughout the detailed circuit descriptions contained in the sections that follow, reference is made to a number of different "building block" submodules. These submodules are members of a family of standard circuits which perform many of the functions required in a receiving system. Each circuit is self-contained in a shielded crystal can enclosure and is designed to work in a 50 ohm system. The functions provided include amplification, phase shift, attenuation, power division, frequency conversion, phase detection, frequency doubling, and r-f signal switching.

The most commonly used building blocks and their salient electrical characteristics are listed below. Maximum power output given for the amplifiers is for 1 dB signal compression.

a) Amplifier, RF-1705

Gain	20 dB
Frequency Range	1-80 MHz
Maximum Output Power	+8 dBm
Noise Figure	8 dB max.

b) Amplifier, RF-1703

Gain(selectable by external connection)	6 dB	12 dB
Frequency Range	5-200 MHz	5-100 MHz
Maximum Output Power	+8 dBm	+14 dBm
Noise Figure	10 dB maximum	

c) Amplifier, RF-1704

Gain	14.5 dB
Frequency Range	1-200 MHz
Maximum Output Power	+8 dBm
Noise Figure	8 dB maximum

d) Amplifier, RF-1706

Gain	26 dB
Frequency Range	0.1-20 MHz
Maximum Output Power	+19 dBm

e) Attenuator, Voltage Controlled (VCA) RF-1710

Attenuation Range	2-30 dB
Frequency Range	10-200 MHz
Maximum Input Power	+5 dBm

f) Phase Shifter, Voltage Controlled (VCØS) RF-1722

Phase Shift Range (for 1 to 15 VDC)	200 degrees minimum
Bandwidth	±10% of center frequency
Available Center Frequencies	10, 50, 110 MHz
Insertion Loss	10 dB maximum

g) Hybrid Power Divider, RF-1715

Frequency Range	2-200 MHz
Insertion Loss (including power division)	3.3 dB max., 2-100 MHz 3.8 dB max., 100-200 MHz
Isolation (between output ports)	30 dB minimum

h) Quadrature Hybrid, RF-1717

Frequency Range	10 ± 1 MHz
Phase shift between outputs	90 ± 2 degrees
Insertion loss (including power division)	3.5 dB maximum
Isolation (between output ports)	30 dB

i) Frequency Doubler, RF-1730

Frequency Range (input)	1 - 100 MHz
Insertion Loss (+7 dBm in)	12 dB
Fundamental and 3rd harmonic suppression	25 dB minimum

j) Phase Detector, RF-1735

Operating Frequency	10 MHz
Reference drive level	+19 dBm
D-C Offset	5 mv maximum
Sensitivity (-13 dBm input signal)	250 mv/rad
Maximum input level (1 dB compression)	+13 dBm

k) Directional Coupler, RF-1718

Frequency Range	10-300 MHz
Insertion Loss	1.8 dB maximum
Coupling	10 \pm 0.5 dB
Directivity	25 dB minimum

l) RF Detector, RF-1736

Frequency Range	2-150 MHz
Output Level	3 VDC minimum
Required RF Input Level	-17 dBm, 2-50 MHz
	-9 dBm, 50-150 MHz

m) Variable Pad, RF-1713

Attenuation Range	9 dB
Frequency Range	10-120 MHz
Impedance	50 ohms nominal
	VSWR <1.5:1

n) SPST Switch, RF-1741

Frequency Range	5-200 MHz
Isolation	>60 dB 5-100 MHz
	>50 dB 100-200 MHz
Insertion Loss	<1.0 dB

o) SPDT Switch, RF-1742

Frequency Range	5-200 MHz
Isolation	>40 dB, 5-75 MHz
	>30 dB, 75-200 MHz
Insertion Loss	<1.0 dB

p) 20 dB Switch, RF-1745

Frequency Range	5-120 MHz
Switched Attenuation	20 dB \pm 1 dB
Minimum Attenuation	<1.0 dB

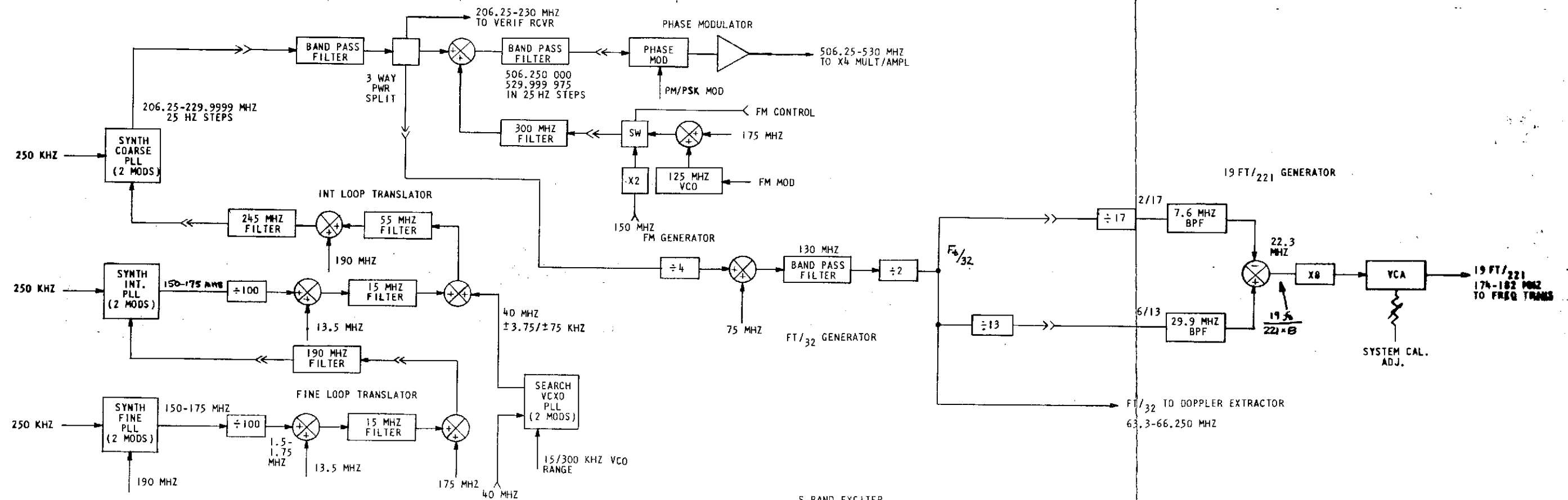
3.2 Exciter Subsystem

The exciter subsystem generates the drive signal for the antenna-mounted S-Band Multiplier/Amplifier at one-fourth the final frequency. The X4 multiplier accepts the 506.250,000 to 529.999,975 MHz, selectable in 25 Hz steps, from the exciter and generates the required 2025.000 to 2119.999,900 MHz signal with 100 Hz increments. A frequency synthesis diagram for the exciter is shown in Figure 3.2.1. The various reference frequencies indicated on the diagram are derived from a highly stable 5 MHz internal standard or, alternately, from a 1 or 5 MHz external standard.

The major outputs from the exciter are the 506.25 to 530 MHz modulated signal, the $f_T/32$ unmodulated output to the doppler extractor, the 206.25 to 230 MHz synthesizer output to the Verification Receiver, and the $19f_T/221$ output to the Frequency Translator.

The 25 Hz incremental tuning over the 506.25 to 530 MHz band is provided by three separate synthesizer phase lock loops. The "coarse" loop moves in 250 kHz increments over the 24 MHz band. The outputs from the "intermediate" and "fine" loops provide the 2.5 kHz and 25 Hz interpolative increments, respectively. The design of the three loops is identical, so that the modules which comprise each loop are physically interchangeable. This synthesizer design is essentially the same as that used in the MFR systems. The phase noise performance of the synthesizer is discussed in Section 4.1.

The VCXO search capability is provided by a forcing signal fed into the coarse loop. This approach provides additional



S-BAND EXCITER
FREQUENCY SYNTHESIS DIAGRAM
FIGURE 3.2.1

filtering of the VCXO signal by the synthesizer loop, as well as integrating the search frequency variation into the synthesizer output. The advantage of this latter feature is that the output signal to the Verification Receiver and the $f_T/32$ output used in generating the local oscillator for the 240/221 Frequency Translator are precise even when the search oscillator is not phase locked.

The test sweep mode is implemented in this design by disabling the coarse loop and sweeping the VCO over its tuning range.

As indicated in Figure 3.2.1 the $f_T/32$ frequency is derived by dividing the synthesizer output signal by four and mixing with one-fourth of the side-step reference frequency ($300/4 = 75$ MHz). Subsequent division by two results in the desired $1/32$ of the final transmit frequency.

The FM information is introduced on the 300 MHz injection frequency at the final mixer in the exciter. The selection of these frequencies was carefully considered in order that harmonics and undesired sideband products from this mix not appear in the 2200-2300 MHz band. For example, any modulation injection frequency between 80 MHz and 275 MHz can result in a spurious sideband on the 2025-2120 MHz transmit signal which falls within the 2200-2300 MHz "forbidden" band.

PM and PSK modulation is performed directly at the final exciter frequency, preceding the times four multiplier.

3.2.1 Synthesizer

The synthesizer used to generate the S-Band transmit signal covers the frequency range of 206.250,000 to 229.999,975 MHz in 25 Hz increments. Subsequent multiplication by a factor of four provides the specified 100 Hz steps.

As shown on Figure 3.2.2 the synthesizer makes use of three essentially identical "divide-and-lock" phase lock loops. Each loop covers two decades of frequency range at the final S-Band frequency. The "fine" loop provides 100 Hz and 1 kHz steps, the "intermediate" loop provides 10 kHz and 100 kHz steps, and the "coarse" loop provides 1 MHz and 10 MHz steps.

Particular attention is paid to optimizing the bandwidth of the loop and to decoupling of the power supply so as to meet both the specified phase noise and spurious response requirements. These areas are analyzed in Section 4.

The core of the design is in the three phase locked VHF oscillators. The output of each oscillator is controlled in 250 kHz increments by means of a programmed divider. To obtain the necessary finer increments the "intermediate" and "fine" VCOs are divided by 100. High speed emitter-coupled logic (MECL III) is used to accomplish the division. A single MSI integrated circuit (MC1678L) is used to accomplish the initial divide-by-10 in this divider. The divided down VCO outputs in the range of 1.50 to 1.75 MHz are translated up to VHF frequencies in steps chosen for low spurious product generation.

The critical voltage controlled oscillator circuit in the synthesizer phase lock loops uses a low noise J-FET operating

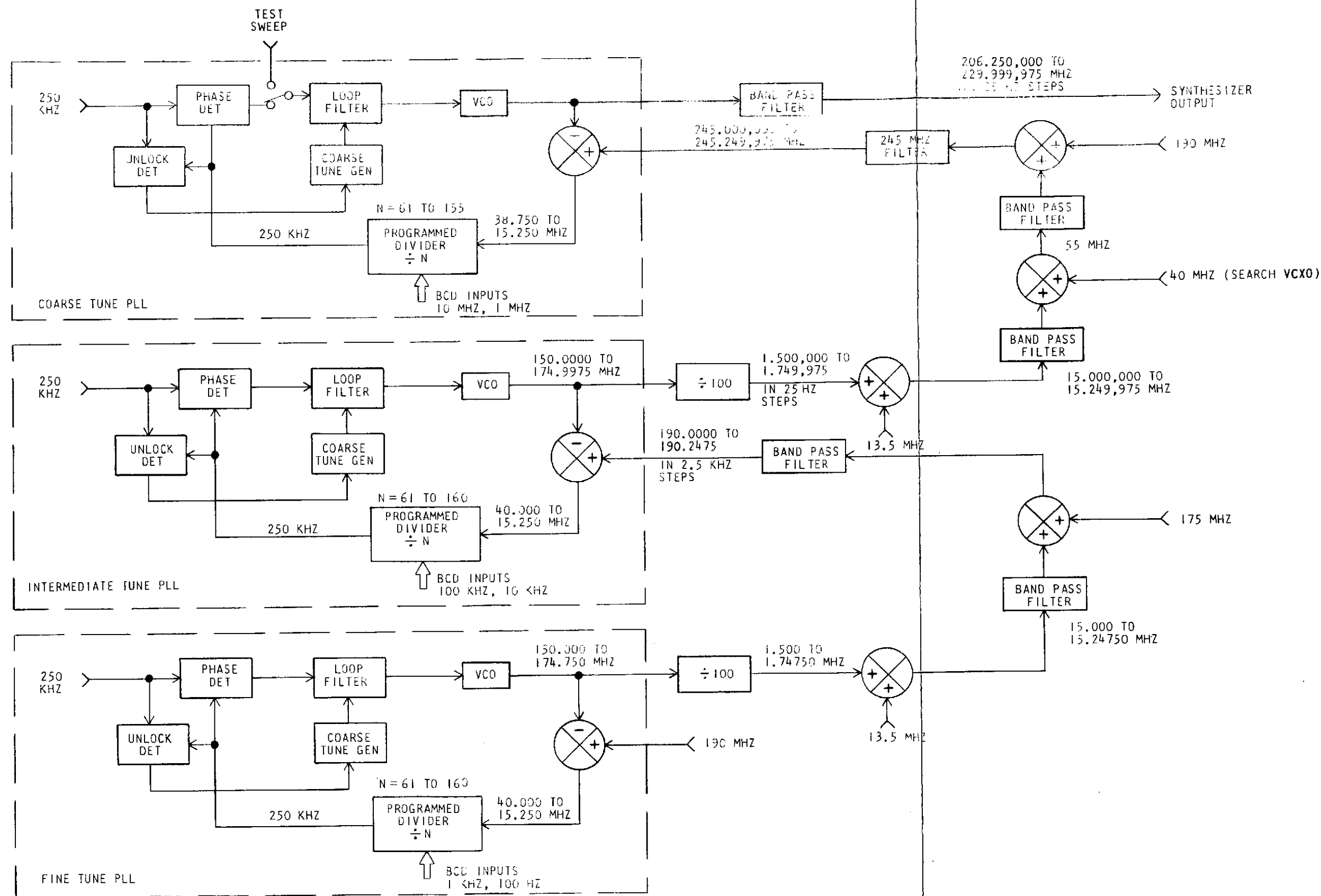


FIGURE 1-1

WOLDOOT FRAME 1

WOLDOOT FRAME 2

in the common gate mode. The oscillator mechanical construction is extremely rugged to reduce microphonics to a negligible level.

The programmed divider utilizes high speed Schottky-clamped TTL logic which typically toggles at a 100 MHz rate. The program inputs are BCD (four line 1-2-4-8 code) supplied from the Exciter Control. The variable divide ratio (61 - 161) causes the loop gain to vary by a factor of 2.6:1. This is compensated by the VCO sensitivity which varies in an approximate inverse manner.

A sample and hold phase detector is used because of its inherent capability for minimizing spurious products generated by the phase detector reference frequency. Techniques are used to obtain excellent reference rejection such as: the use of a high speed MOS FET sampling switch with low leakage; shutting off the ramp at the sampling instant to reduce reference frequency ripple on the storage capacitor; adjustable capacitive "bucking" to cancel sampling pulse energy which might otherwise appear at the phase detector output due to stray coupling. These measures reduce the reference spurious sidebands on the synthesizer output to greater than 80 dB below the desired signal.

The loop filter is a high gain active integrator employing lag-lead compensation to control the loop response. Since the lag-lead network has two independent time constants the natural frequency and damping can be controlled independently. Then, the low frequency loop gain can be high, to track out low frequency phase noise, and the loop can also be slightly

overdamped to provide good stability and minimize high frequency noise.

An unlock detector is used in each loop to indicate when the VCO is not phase locked. The output of the unlock detector drives a coarse tune generator which sweeps the VCO to within the acquisition bandwidth of the phase lock loop. Typical acquisition time, after a frequency change, is less than 5 milliseconds. The unlock detectors are "or"ed together in order to light a front panel indicator on both the local and remote control panels.

The synthesizer comprises eight circuit modules. They are:

- 1) Three identical VCO modules
- 2) Three identical $\pm N$ /Phase Detector modules which contain the programmable divider, phase detector, unlock detector and the coarse tune generator.
- 3) One "fine" loop translator module, in which the output of the fine loop is divided by 100 and translated up to 190 MHz.
- 4) One "intermediate" loop translator module, in which the output of the "intermediate" loop is divided by 100 and translated up to 245 MHz.

3.2.1.1 Synthesizer VCO Modules

The synthesizer VCO module contains the lag-lead loop filter required by the second order loop, the VCO, and the VCO frequency to 15 - 40 MHz mixing circuit. The input control voltage for the VCO is supplied by the loop sample-and-hold phase detector and the coarse tune generator. The VCO output is supplied to the synthesizer up converter (coarse VCO) or to the +100 circuit in the frequency translation modules (fine and intermediate VCOs). A functional block diagram of this module is shown in Figure 3.2.3.

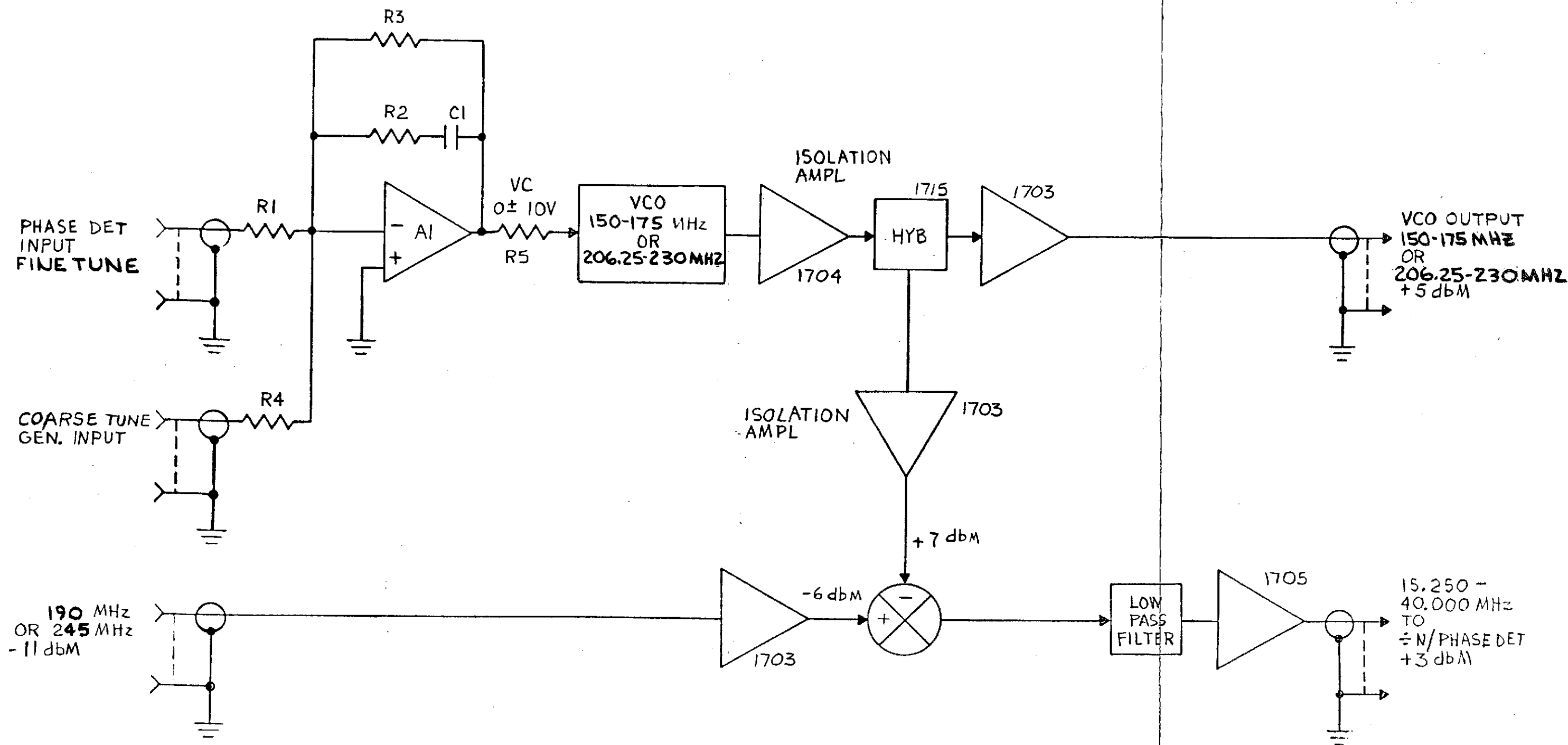
The loop filter circuit comprises operational amplifier A1 and filter components R1, R2, R3 and C1. The ratio R3/R1 establishes the static loop gain and if $R_3 \gg R_1 \gg R_2$, which is the case, the transfer function of the loop filter reduces to:

$$F(s) = \frac{sCR_2 + 1}{sCR_1} \text{ or } F(s) = \frac{sT_2 + 1}{sT_1}$$

The time constants T1 and T2 establish the loop natural frequency and damping.

The VCO is controlled by the output of the loop filter, isolated by R5. The basic oscillator is a low-noise J-FET operating in the common gate configuration. The drain circuit is tuned by back-to-back voltage-variable capacitors to cover the required 25 MHz range.

The oscillator is buffered and supplied as an output and is also converted to the 15 - 40 MHz range by means of a difference mix with 190 or 245 MHz. The 15 - 40 MHz signal is supplied to the programmable divider.



SYNTHESIZER VCO MODULE
FIGURE 3.2.3

3-15

FOLDOUT FRAME 1

FOLDOUT FRAME 2

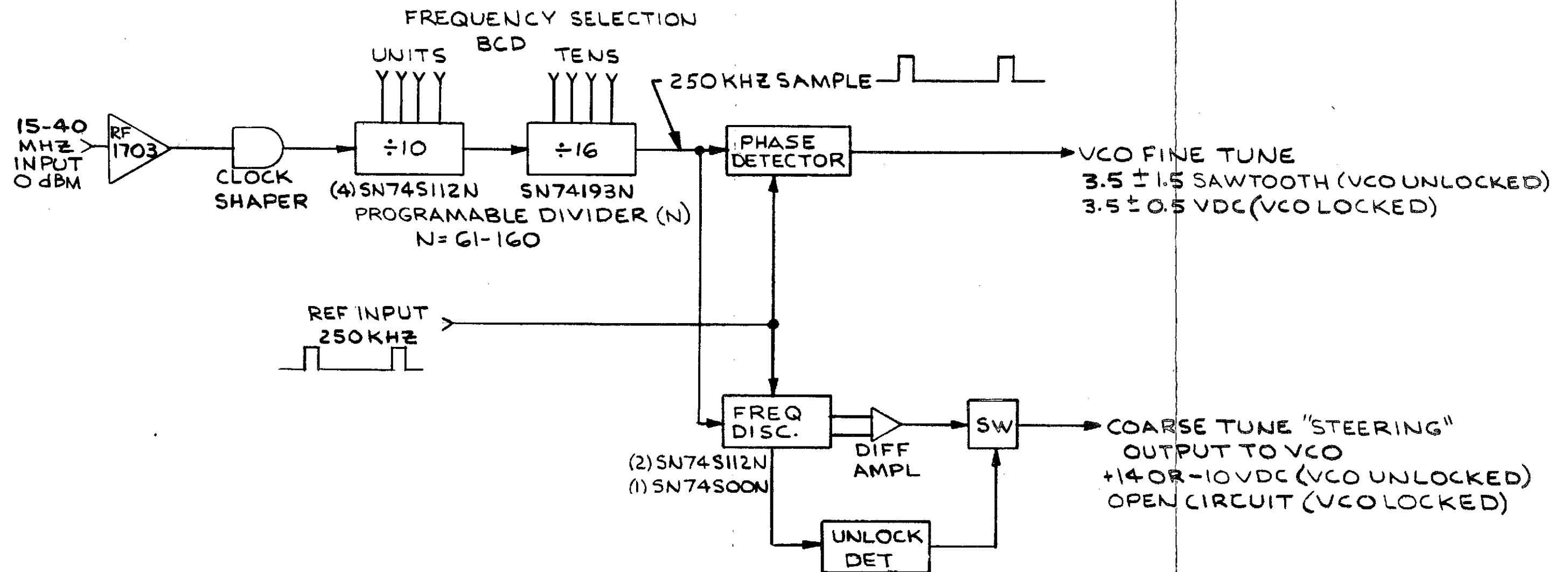
3.2.1.2 Programmable Divider/Phase Detector

The synthesizer programmable divider/phase detector module contains all the digital and switching circuitry needed to control the phase-lock loops. The circuitry is broken down into three main areas: the programmable divider, the sample-and-hold phase detector, and the unlock detector/coarse tune generator.

A block diagram of the divide-by-N Module is shown in Figure 3.2.4. The programmable divider is required to accept inputs in the 15.250 to 40 MHz frequency range and divide these frequencies to a constant 250 kHz output to provide sample pulses to the phase detector. The divider must be able to divide by any integer from 61 to 160 selectable by inputs from the Exciter Control.

The divider is composed of a divide-by-ten counter, a divide-by-sixteen counter, and a preset counter. The divide-by-ten and preset counter are made up of high-speed, Schottky-clamped TTL dual J-K flip-flops designed to handle clock speeds in excess of 50 MHz. The divide-by-sixteen counter is an integrated circuit synchronous binary counter subsystem.

The divide-by-ten counter followed by a divide-by-sixteen counter is capable of counting up to 160 clock pulses. That is, the counter is "full" after 159 pulses and recycles to zero on the 160th pulse. The counters also have the additional feature of being able to be preloaded. Preloading is a technique whereby a counter can be advanced to a given state initially so that fewer input pulses are needed to produce a full count condition.



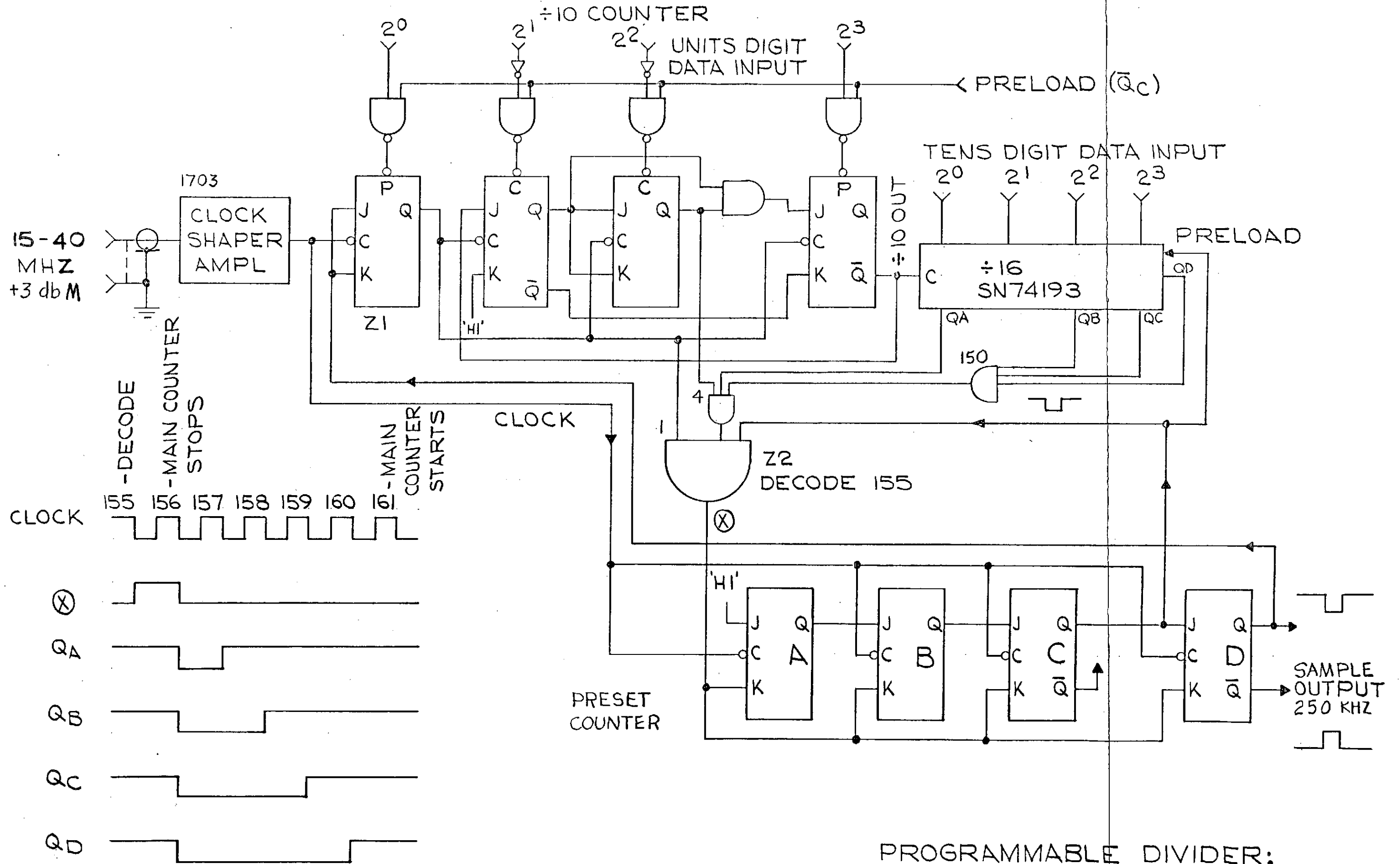
DIVIDE-BY-N MODULE

The frequency control lines from the Exciter Control preload the counter after each reset cycle. For example, if "99" is preloaded into the counter, the counter provides an output after 61 clock transitions have occurred.

The preset counter is used to store a fixed number of input pulses while the +10 and +16 counters are being preloaded.

The divider operation can be understood by referring to the logic diagram and timing diagram of Figure 3.2.5. Assume that initially the +10 and +16 counters are in the "zero" state and that Q_A , Q_B , Q_C and Q_D are in the "one" state. After 155 pulses have occurred (the J-K flip-flops are triggered on the trailing edge of the clock pulse), this state is sensed by "AND" gates, Z2. The output of Z2 sets the "K" inputs of the preset counter to "1", enabling this counter. On the trailing edge of the next clock pulse, 156, the "Q" outputs of the preset counter go to "zero" state. The Q_D output is applied to the J-K inputs of Z1 disabling the +10 and +16 counters. At the same time Q_C and $\overline{Q_C}$ enable the preset lines and digit information is loaded into the counters. After four more pulses (trailing edge of the 160th pulse), the preset counter returns to its initial state, enabling the +10 and +16 counters, and normal count-up from the preset state occurs.

The preset counter is necessary to allow enough time to preload digit information into the +10 and +16 counters. The output, Q_C , is used to enable the preset lines to the +16 counter and to insure that decode gate, Z2, is disabled prior to the third pulse into the preset counter. The $\overline{Q_C}$ output



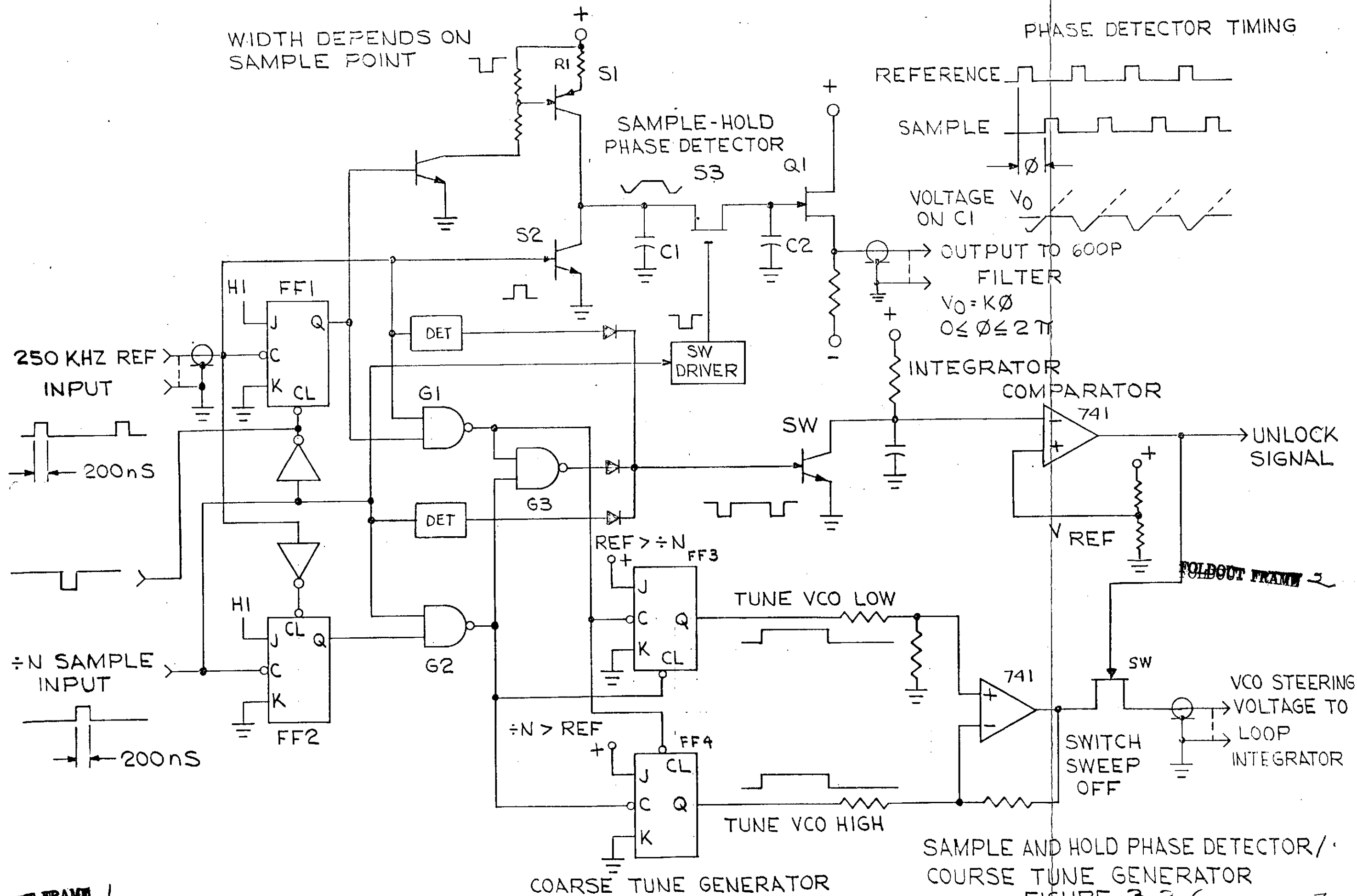
TIMING DIAGRAM

PROGRAMMABLE DIVIDER;
FUNCTIONAL BLOCK DIAGRAM
FIGURE 3.2.5

enables the preset lines to the +10 counter. The sample output is taken from \overline{Q}_D , minimizing the delay from the clock input to output thereby insuring low jitter.

The sample and hold phase detector is shown in Figure 3.2.6. The phase detector comprises ramp generator (Q1, R1, C1), sample switch, S3, and hold capacitor, C2. The phase detector receives two inputs; a reference signal consisting of narrow pulses occurring at a repetition rate of 250 kHz, and a sample signal consisting of narrow pulses at a rate determined by the VCO frequency and divider ratio. The sample rate is exactly 250 kHz when the VCO is locked. The phase detector generates a voltage which is linearly related to the phase difference between the reference and the sample pulses.

By referring to the timing diagram on Figure 3.2.6 the operation of the phase detector can be understood. Flip-flop, FF1, is set to the "1" state on the negative edge of the reference pulse. This causes switch, S1, to close and the sawtooth is generated by charging capacitor, C1, through transistor, Q1. At the occurrence of the sample pulse, FF1 is cleared and sample switch, S3, is closed. This action also causes switch, S1, to open and the ramp is held to its value at the sample time. During the sampling interval the voltages on capacitors, C1 and C2 equalize. If C1 is much larger than C2, the voltages equalize to a value very close to that on C1 when the sample was taken. After the sample pulse, switch S3 is opened and the voltage is stored on capacitor C2 until the next sample pulse occurs. The ramp capacitor, C1, is discharged on the next positive reference pulse and the cycle is complete.



This method of turning off the ramp generator during the sample period prevents the voltage on C1 from changing and appearing as ripple on the holding capacitor, C2. Source follower Q2 provides a high impedance load to capacitor C2 so that it does not discharge between sample pulses. When the loop is in lock, the voltage across capacitor C2 will remain nearly constant, changing only by the amount necessary to correct for VCO phase drift. However, when the loop is not locked, the sawtooth will be sampled at a slightly different point during each interval. The resultant voltage on capacitor C2 will be a reconstructed sawtooth with a repetition rate equal to the difference between the reference and the sample rate.

Figure 3.2.6 also illustrates the unlock detector and coarse tune generator. The unlock detector utilizes a frequency discriminator comprising flip-flops, FF1 and FF2 and "NAND" gates G1, G2, and G3. The criterion for determining out-of-frequency-lock is when the negative going edges of the sample and reference pulses do not occur alternately in time as they do when the loop is locked. When an out-of-frequency condition exists, in which the reference frequency is higher than the sample frequency, the negative edge of the reference pulse will set flip-flop, FF1 to a logical "1" state. The next reference pulse will then be gated through "NAND" gate, G1. In the locked condition, the sample pulse would have cleared the flip-flop before the occurrence of the second reference pulse, preventing any pulses from getting through. Flip-flop, FF2, and gate, G2, work in a similar manner to

detect when the sample rate is greater than the reference rate. Therefore, the discriminator supplies a series of pulses from either G1 or G2 (never both) depending on whether the reference rate is greater than or less than the sample rate, respectively.

The outputs of "NAND" gates, G1 and G2, are combined in "NAND" gate, G3. The output of G3 consists of a series of pulses occurring at a rate equal to the difference between the sample and reference rates. This difference frequency is integrated and compared to a fixed reference. Detectors are included to indicate the absence of the reference pulses or sample pulses and also cause the unlock detector to operate. The integrator thus provides a DC voltage proportional to this frequency difference. The comparator is set to trip when the difference exceeds 10 kHz (the lock-in range of the loop).

Steering voltages for the VCO are supplied from gates G1 and G2 and flip-flops, FF3 and FF4. The outputs of the flip-flops steer the VCO toward the correct frequency. The duration of the steering signal is controlled by the unlock detector. Therefore, when the loop is within its capture range, detected by the unlock comparator, the sweep voltage is removed.

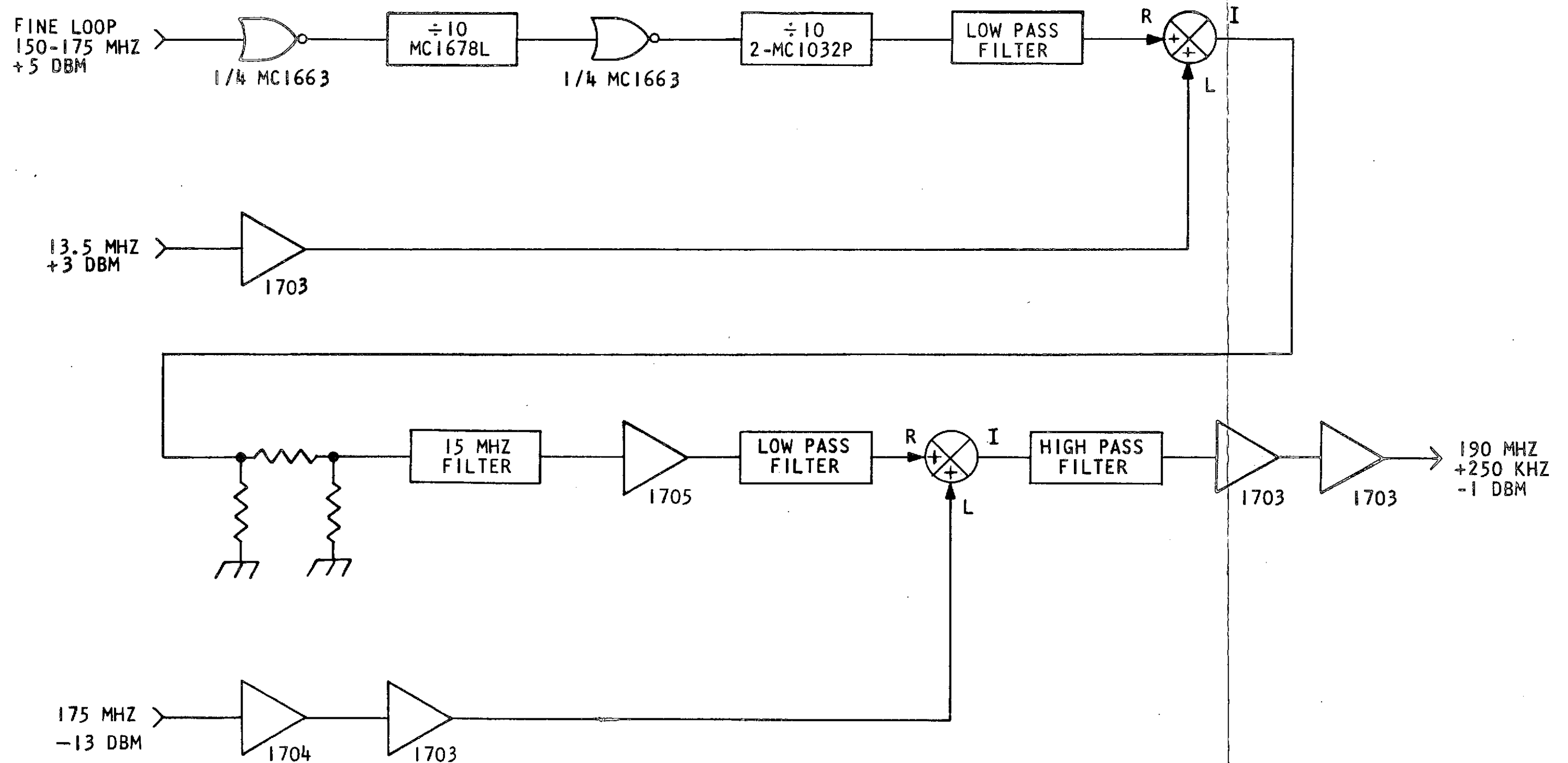
3.2.1.3 Fine Loop Translator Module

This module accepts the 150 to 175 MHz signal from the fine VCO phase-lock loop, divides it by 100 to provide 2.5 kHz steps, and translates it to 190.000 to 190.250 MHz by means of a double conversion. A block diagram of this module is shown in Figure 3.2.7.

The 150 to 175 MHz signal is shaped by NOR gate Z1 and applied to the input of the divide-by-10 circuit. The shaping gate is a high speed Motorola MECL III gate. The divide by 10 circuit, Z2, is a Motorola MC1678L decade counter capable of dividing frequencies up to 325 MHz. The output of the +10 counter drives the second decade counter, Z4.

The 1.5 to 1.7475 MHz is filtered and converted to 15.0 to 15.250 MHz by means of a sum mix with 13.5 MHz. The mixer balance and the narrowband filter following it reduce the 13.5 MHz signal to more than 80 dB below the desired output.

The final output of 190.000 to 190.250 MHz is obtained by means of a sum mix with 175 MHz. This output is supplied to the intermediate VCO through a narrowband tubular bandpass filter which rejects the 175 MHz signal. The filter is external to the module.



FINE LOOP TRANSLATOR
FIGURE 3.2.7

3.2.1.4 Intermediate Loop Translator Module

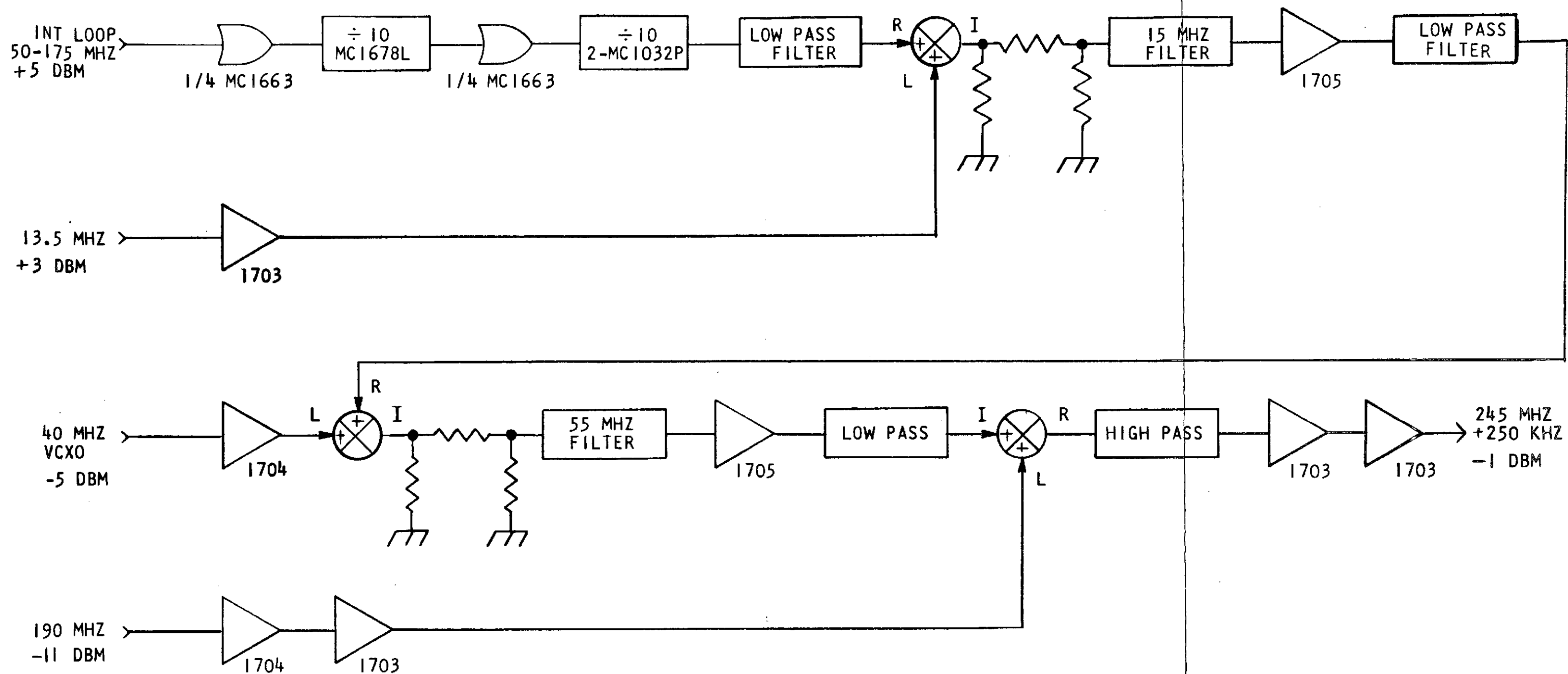
This module accepts the 150 to 175 MHz signal from the "intermediate" VCO phase-lock loop, divides it by 100 to provide 2.5 kHz steps, and translates it to 245.000 to 245.250 MHz by means of a triple conversion. A block diagram of this module is shown in Figure 3.2.8.

The 150 to 175 MHz signal is shaped by NOR gate Z1 and applied to the input of the divide-by-10 circuit. The shaping gate is a high speed Motorola MECL III gate. The divide by 10 circuit, Z2, is a Motorola MCL678L decade counter capable of dividing frequencies up to 325 MHz. The output of the +10 counter drives the second decade counter, Z4.

The 1.5 to 1.7475 MHz is filtered and converted to 15.0 to 15.250 MHz by means of a sum mix with 13.5 MHz, identical to the Fine Loop Translator.

The 15 MHz is converted to 55 MHz by means of a sum mix with the 40 MHz search VCXO signal. Mixer balance and the 55 MHz filter remove the 40 MHz signal.

The final output of 245 to 245.250 is obtained by a sum mix of the 55 MHz and a 190 MHz reference signal. The resultant 245 MHz signal is supplied to the coarse VCO phase locked loop through a narrowband tubular bandpass filter. The filter is external to the module.



INT LOOP TRANSLATOR
FIGURE 3.2.8

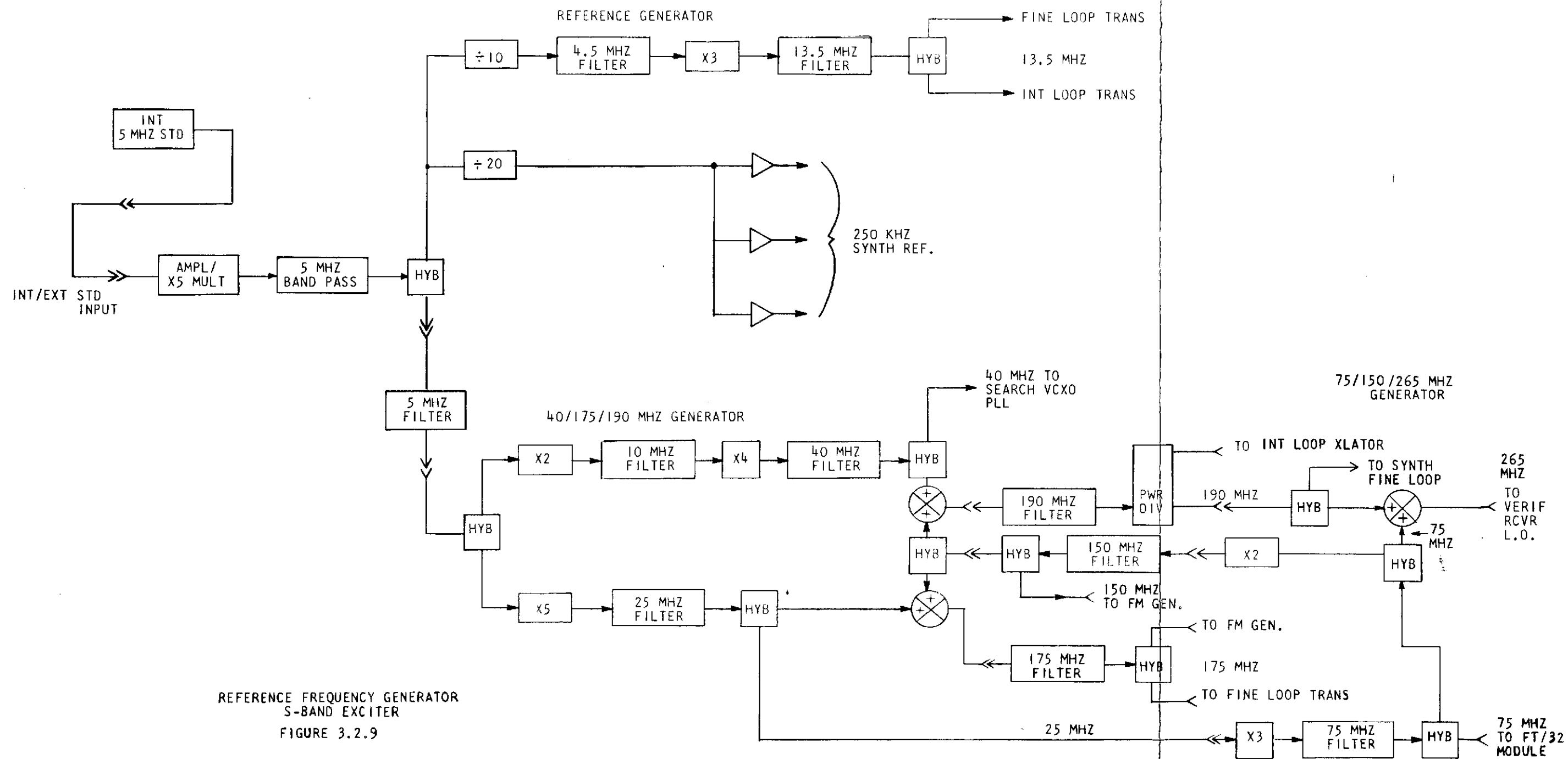
3.2.2 Reference Frequency Generation

The different reference frequencies required in the synthesizer are all derived coherently from the frequency standard signal. Figure 3.2.9 details the methods used to generate these frequencies. The techniques suggested therein are not new or novel, and have been used by RFC in numerous other equipments, including the Multifunction Receivers. The two major criteria in the design of these circuits are to provide signals which are sufficiently spurious-free to meet the 60 dB spurious output specification and to preserve the excellent phase noise spectral density qualities of the frequency standard.

Spurious-free performance is obtained by the simple application of good packaging and filtering techniques. Care is taken with the mounting and shielding of band-pass filters in order that the full ultimate attenuation characteristics of the filters are not compromised by stray coupling.

Phase noise characteristics for the generated reference signals are commensurate with the frequency standard if certain precautions are observed in the design of the multipliers. All frequency multipliers are operated at high signal levels to prevent the circuit "noise floor" from degrading the phase noise density of the standard. Also, a narrowband crystal filter is placed between the frequency standard and the multipliers to improve the phase noise density of the standard. The filter has a 3 dB bandwidth of less than 400 Hz and effectively removes noise components 200 Hz and beyond.

Selection of the internal or external standard is



REFERENCE FREQUENCY GENERATOR
S-BAND EXCITER
FIGURE 3.2.9

accomplished through a manual patch made at the rear of the exciter drawer. The frequency standard signal is passed through a limiting amplifier and filter circuit, so that the frequency may be either one or five megahertz.

Three modules generate the reference signals required by the exciter system. These signals are:

1. 250 kHz - Three signals used as references for the synthesizer loops.
2. 13.5 MHz - Two signals used for translating the intermediate and fine synthesizer loops to VHF.
3. 40 MHz - One signal used as a reference for the search VCXO phase locked loop.
4. 75 MHz - One signal used as a reference to generate the $f_T/32$ doppler output signal.
5. 150 MHz - One signal used in PM or PSK mode to generate 300 kHz to up-convert the 206.25 to 230 MHz synthesizer signal to 506.25 to 530 MHz.
6. 175 MHz - Two signals, one used to up-convert the synthesizer fine loop to 190 MHz and one to up-convert the FM generator to 300 MHz.
7. 190 MHz - Two signals used to convert the synthesizer fine and intermediate loops to their final VHF frequencies.
8. 265 MHz - One signal used in the Verification receiver local oscillator generation.

3.2.2.1 Frequency Standard

The frequency standard chosen for the S-Band Exciters is the same one used in the Multifunction Receivers currently being built for GSFC under Contract No. NAS5-20473. A copy of the salient specifications of this standard appears in Appendix A.

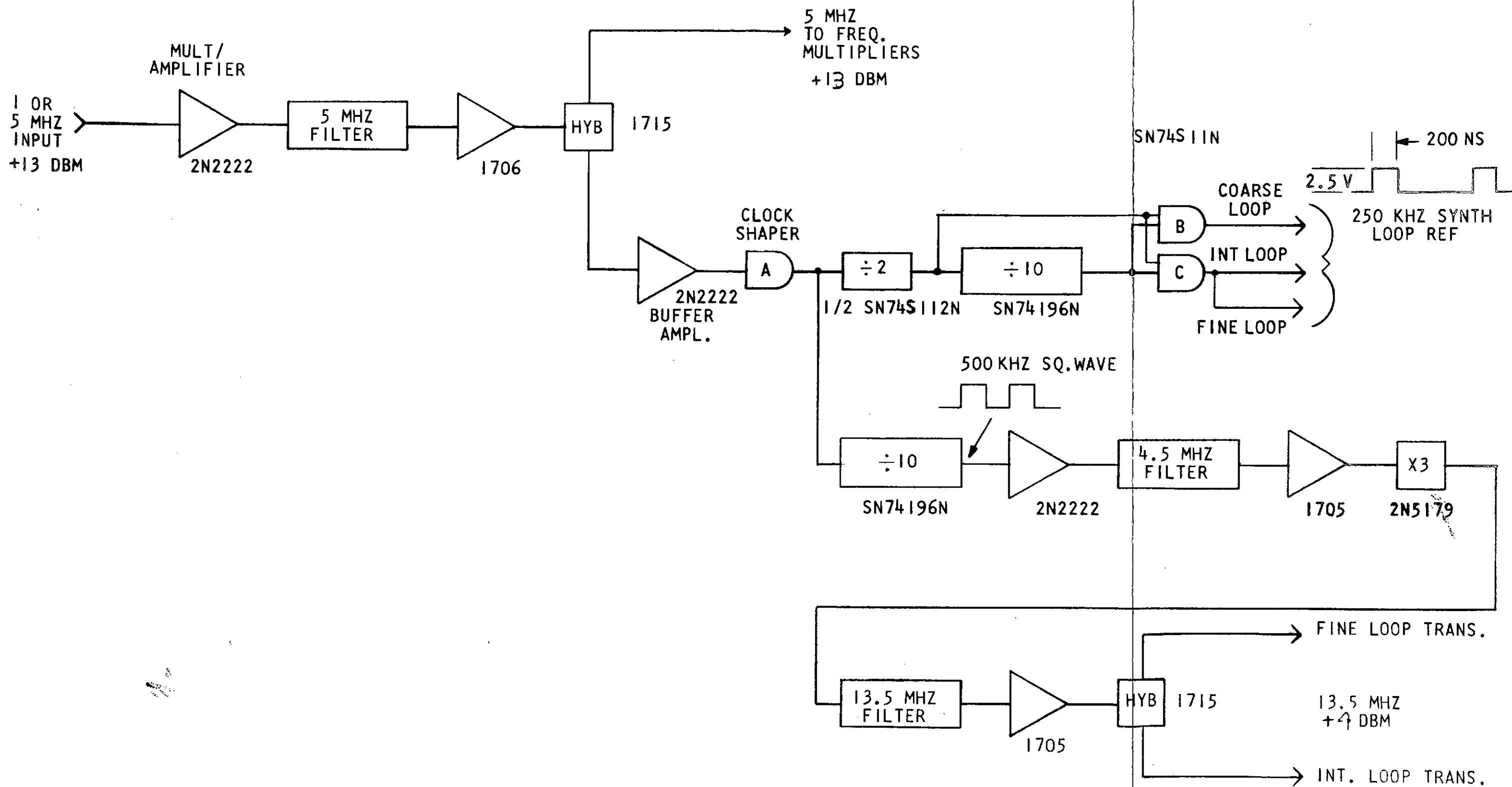
A narrowband crystal filter is used in series with the standard to insure that the integrated phase noise density at S-Band will be commensurate with the 1.0 degree rms phase noise specification. The phase noise specification is analyzed in Section 4.1 of this design evaluation report.

3.2.2.2 250 kHz/13.5 MHz Generator

This module accepts a 1 or 5 MHz frequency standard signal at +13 dBm nominal and provides 5 MHz out to the frequency multipliers, 250 kHz to the synthesizer loops, and 13.5 MHz to the synthesizer loop translators. A detailed block diagram is shown in Figure 3.2.10. The frequency standard signal is amplified and limited to produce 5 MHz when the standard is 1 or 5 MHz. A four section bandpass filter provides 60 dB rejection to the 1 MHz sidebands. Additional filtering is provided by a chassis mounted filter before additional multiplication takes place.

The 5 MHz signal is also divided by 20 to provide 250 kHz pulses to the synthesizer phase lock loops. The first flip-flop in the divider gates the output to provide the proper pulse width and to minimize phase jitter by reducing the total delay through the divider.

A separate "divide-by-ten" circuit provides a 500 kHz square wave. The ninth harmonic, 4.5 MHz, is selected by a four section filter which provides over 40 dB rejection to the 500 kHz sidebands (even harmonics are suppressed in the square wave). The 4.5 MHz signal is tripled to 13.5 MHz and filtered to provide an additional 40 dB rejection to 500 kHz sidebands. This 13.5 MHz signal is provided to the synthesizer loop translator.



REFERENCE GENERATOR
250 KHZ/13.5 MHZ
FIGURE 3.2.10

3.2.2.3 40/175/190 MHz Generator

This module accepts a 5 MHz and 150 MHz input and provides reference outputs of 175 and 190 MHz to the synthesizer and 40 MHz to the search VCXO phase lock loop. A detailed block diagram is shown in Figure 3.2.11. The 5 MHz signal is power divided and supplied to "times five" and "times eight" multipliers.

The "times eight" multiplier comprises a balanced doubler, 10 MHz double tuned filter, a transistor multiplier (X4) and a four section 40 MHz filter. The filter provides 70 dB rejection to the 10 MHz sidebands.

The "times five" multiplier comprises a transistor multiplier and a four section 25 MHz filter which provides 70 dB rejection to the 5 MHz sidebands. A 25 MHz signal output is provided for generation of 75 and 150 MHz.

The 150 MHz signal input is power divided and amplified to provide the local oscillator signal to two double balanced mixers. One mixer sums the 150 and 25 MHz to generate 175 MHz and the other sums 150 and 40 MHz to generate 190 MHz. The mixer outputs are filtered to remove the L.O. and image and then amplified. Tubular bandpass filters located on the main chassis further clean up the 175 and 190 MHz outputs.

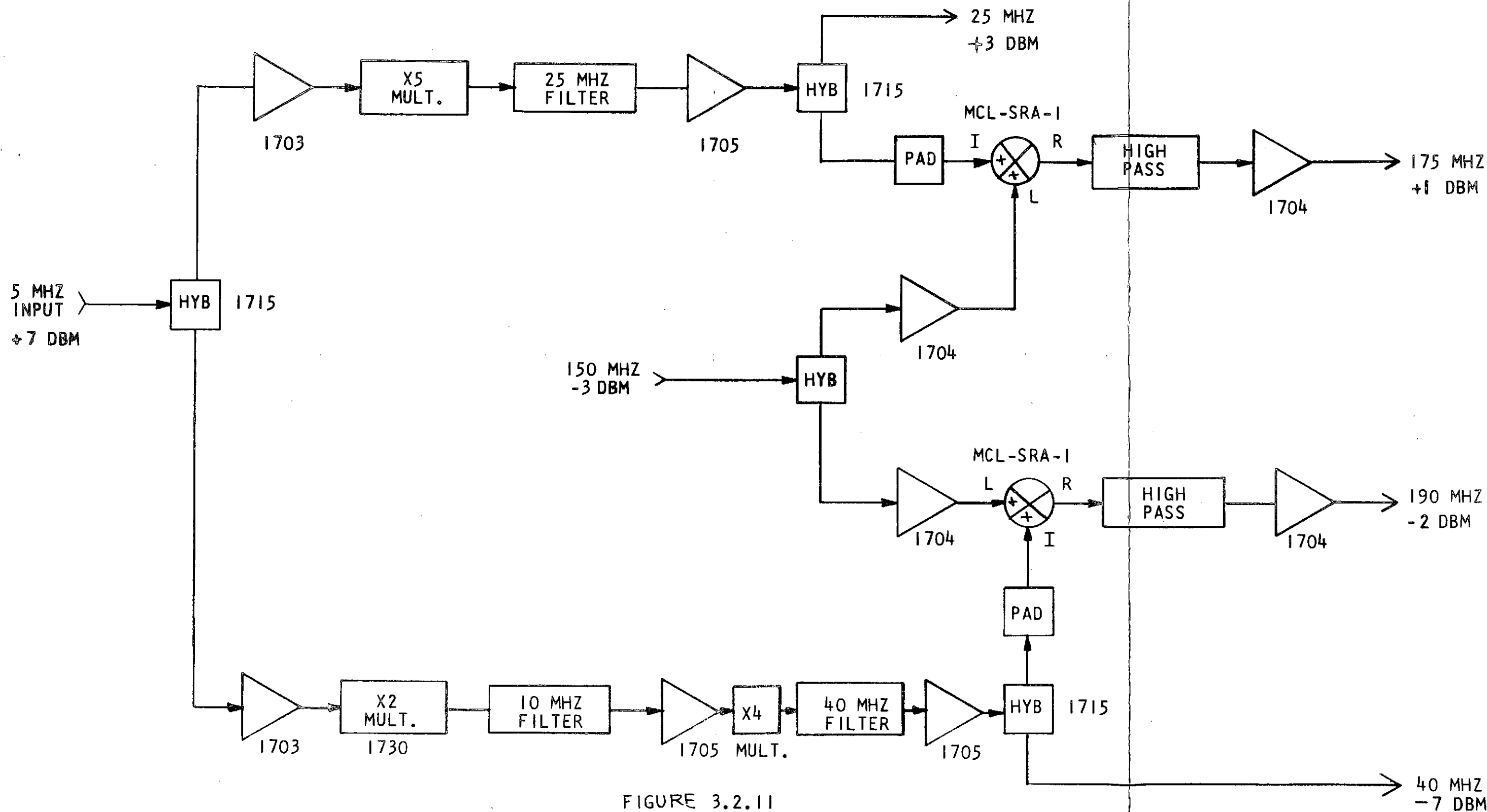


FIGURE 3.2.11
40/175/190 MHz
GENERATOR

3.2.2.4 75/150/265 MHz Generator

This module receives input signals of 25 and 190 MHz and provides outputs of 265 MHz to the Verification Receiver Local Oscillator, 150 MHz to the FM Generator and 75 MHz to the $f_T/32$ doppler output module. A detailed block diagram is shown in Figure 3.2.12.

The 25 MHz signal is multiplied by three to 75 MHz by a transistor multiplier and filtered in a four section filter which attenuates the 5 MHz sidebands by an additional 30 dB. A balanced doubler provides the 150 MHz signal. A tubular bandpass filter mounted on the main chassis removes undesired products.

The 190 MHz input signal and the 75 MHz signal are mixed in a double balanced mixer to produce 265 MHz. The high pass filter at the mixer output removes the image and local oscillator. Additional filtering is provided by a tubular bandpass filter on the chassis.

3.2.3 Search VCXO Module

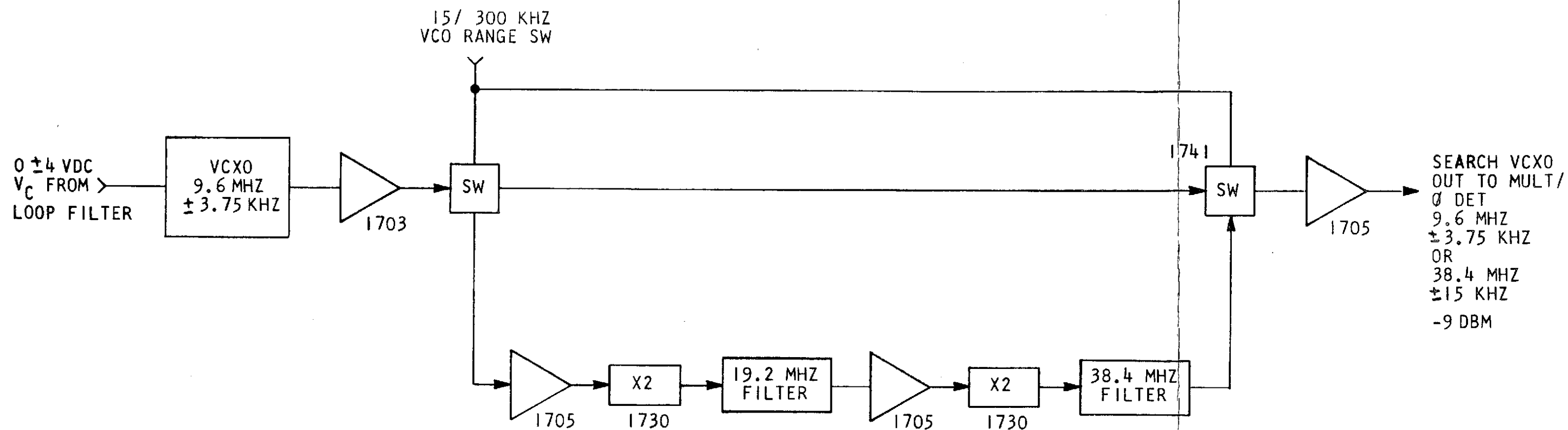
The function of this module is to provide a stable search oscillator for the exciter. The search range is selectable and is either ± 15 kHz or ± 300 kHz. The control voltage for the VCXO is supplied from the loop filter.

Figure 3.2.13 is a functional block diagram of the Search VCXO module. A 9.600 MHz signal is generated by a common gate J-FET oscillator. Feedback from drain to source consists of a series resonant circuit which includes a low spurious fundamental mode crystal and back-to-back voltage-variable capacitors. Adjustments are provided for initially linearizing the control characteristics over a tuning range of 3.75 kHz.

The VCXO output is buffered and supplied to the VCXO Multiplier/Phase Detector for further processing. Two VCO ranges are provided, ± 15 kHz range and ± 300 kHz range. The desired output is selected by PIN diode switches controlled by VCO selection signals from the Exciter Control.

For the 15 kHz range, the buffered VCXO output is supplied directly to the VCXO Multiplier/Phase Detector. The VCXO is multiplied by four to provide an output of 38.400 MHz ± 15 kHz when the ± 300 kHz range is selected.

The times four multiplication is provided by two balanced doubler circuits which inherently provide rejection of the fundamental and third harmonic, thus easing the filter requirements. The outputs of the multipliers are amplified and filtered to reduce the 9.600 MHz sidebands to greater than 70 dB below the desired 38.400 MHz output.



SEARCH VCXO MODULE
FIGURE 3.2.13

FOLDOUT FRAME /

FOLDOUT FRAME 2

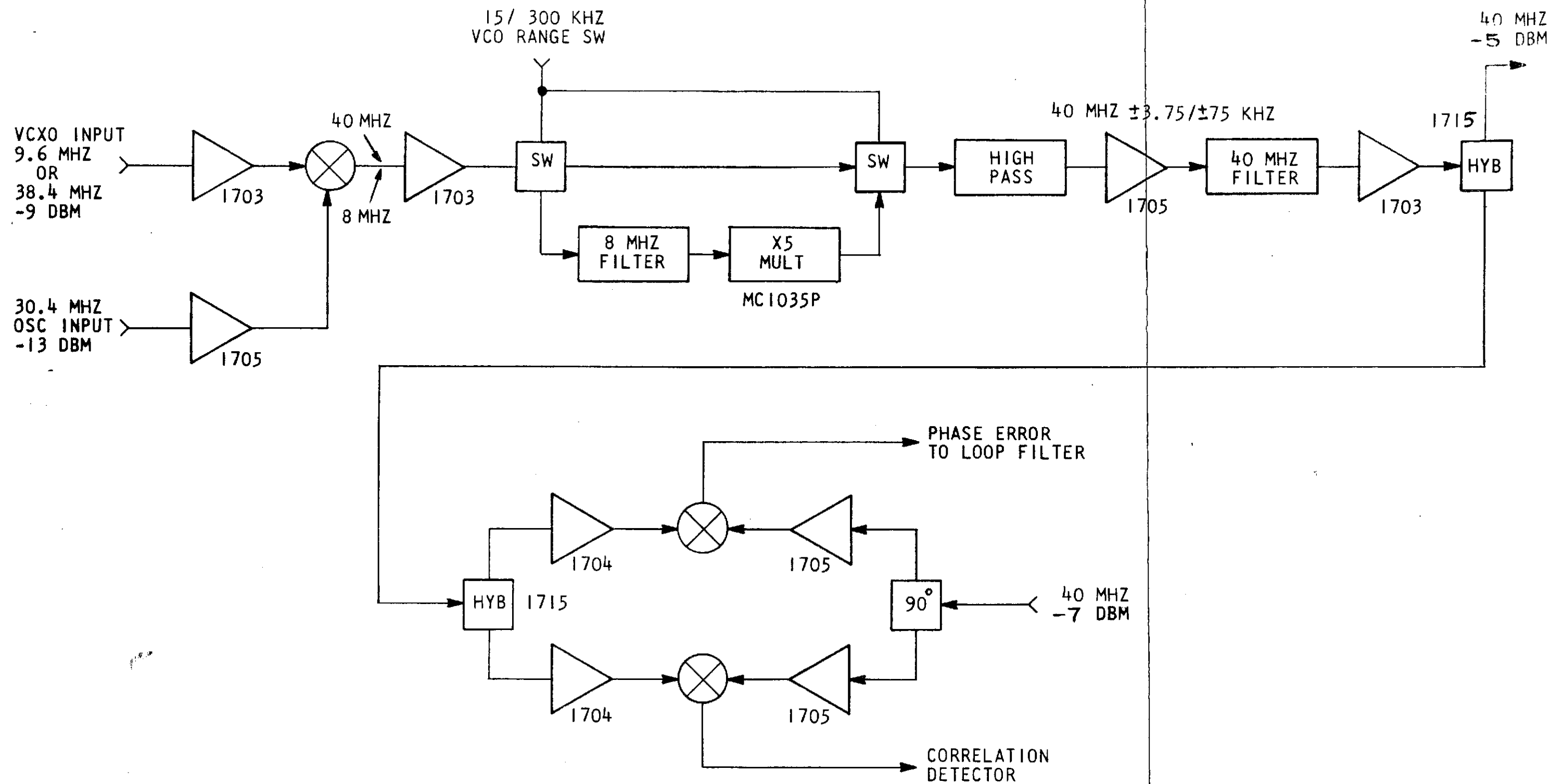
3.2.4 VCXO Multiplier/Phase Detector

The function of this module is to translate/multiply the VCXO to 40 MHz with ± 3.75 or ± 75 kHz search range. Subsequent times four multiplication in the S-Band Amplifier provides the required ± 15 or ± 300 kHz search range. This module also contains the phase detector providing a phase error to the Loop Filter for locking the VCXO in SEARCH OUT mode. A detailed block diagram of this module is illustrated in Figure 3.2.14.

The inputs to the VCXO Multiplier/Phase Detector module are:

- 1) 9.600 MHz ± 3.75 kHz selected by the ± 15 kHz VCO control. This signal is translated to 40.000 MHz by means of a sum mix with 30.4 MHz.
- 2) 38.400 MHz ± 15 kHz selected by the ± 300 kHz VCO control. This signal is down converted to 8.000 MHz by mixing with 30.400 MHz and the difference multiplied by five to give 40.000 MHz ± 75 kHz.
- 3) A crystal oscillator input of 30.400 MHz used to translate the VCXO input of 9.6 MHz or 38.4 MHz to 40 or 8 MHz.
- 4) A coherent 40 MHz signal which is used as a reference input to the phase detector for locking the VCXO.

The critical considerations in the design of this module are to insure a spectrally pure output (spurious level of -80 dB) and to provide sufficient isolation between the different VCXO signal paths (greater than 80 dB). To keep



SEARCH VCXO MULT/
PHASE DETECTOR
FIGURE 3.2.14

spurious mixer products to a minimum, a double-balanced mixer is used and the signal levels are carefully controlled (nominally -10 dBm and +7 dBm). A four-pole filter, common to each VCXO selected, at 40.000 MHz further reduces undesired spurious products to -80 dB. The 8.000 MHz filter in the times five chain reduces the 38.400 MHz adequately so that it does not appear at the output at a level greater than -80 dB.

PIN diode switches are included in the two VCXO signal paths to isolate them from each other. Additional switching is also performed in the search VCXO module as discussed in Section 3.2.3.

The 40 MHz VCXO signal is phase compared to the 40 MHz reference signal in two double balanced mixers. One phase detector provides the phase error voltage to the loop filter. The other, with the reference shifted 90 degrees, becomes a coherent amplitude detector and provides for the lock indication.

3.2.5 Loop Filter/Acquisition Circuits

The Loop Filter PC Board contains the active integrator to phase lock the Search VCXO to the system standard in the "Search OUT" mode. This board also contains the circuitry necessary to implement the search function (Search IN) and to provide the automatic sweep decay when Search OUT is selected. A simplified schematic of the board is illustrated in Figure 3.2.15A. Details of the individual circuits are described below.

1) Phase Lock Loop

The "P" phase detector signal is switched on by Q1 in the Search OUT mode only. Prior to phase lock the signal bypasses Q2 through an RC circuit. After lock has been acquired, switch Q2 closes.

Switches S1 and S2 control the feedback resistors to give three loop bandwidths labeled wide, medium, and narrow. The 10 μ F capacitor is used for all three loop bandwidths.

Amplifier AR1 has 1 M Ω feedback via switch Q3 before lock. This feedback is opened when lock is detected. During lock, then, the DC feedback loop is via the VCXO and "P" phase detector and AR1 is operating at full DC gain.

When operating in the 300 kHz VCXO range mode, the full output of AR1 is applied, via Q4 and voltage follower AR2, to the feedback 10 μ F capacitor. When operating in the 15 kHz VCXO range mode, Q5 switches only 1/20 of the output of AR1 into the AC feedback loop. This results in 20 times the AC gain in AR1. This equalizes the 20 times loss in loop gain in 15 kHz mode. This 20 times loss in gain is caused by

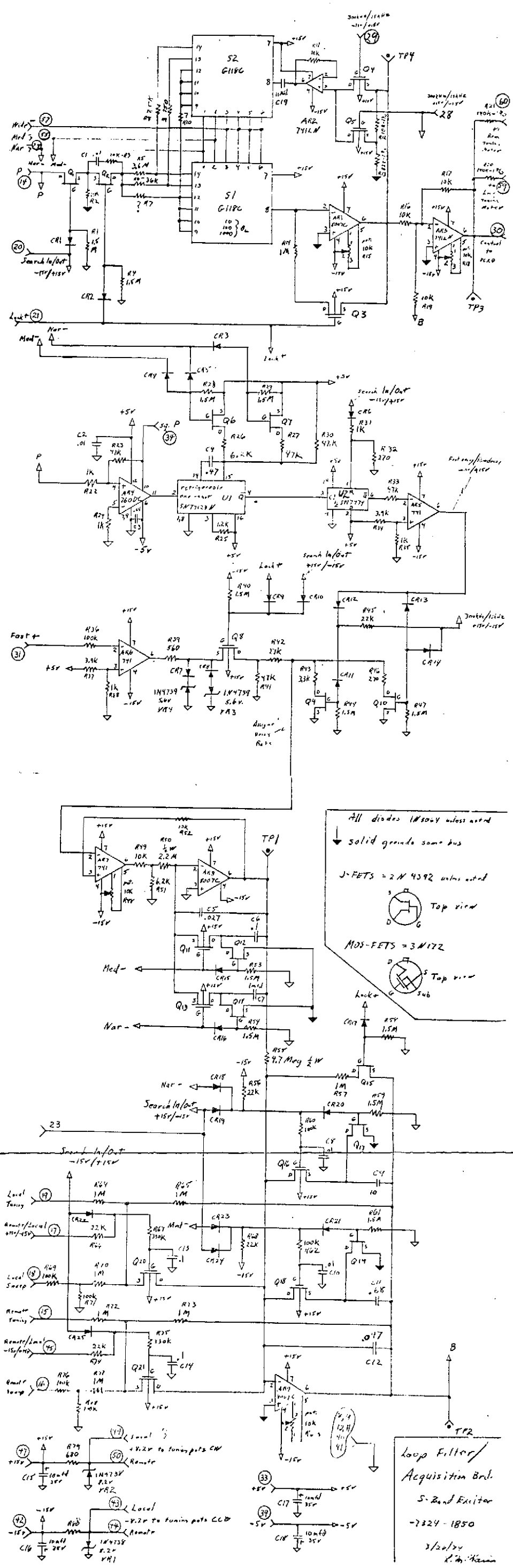
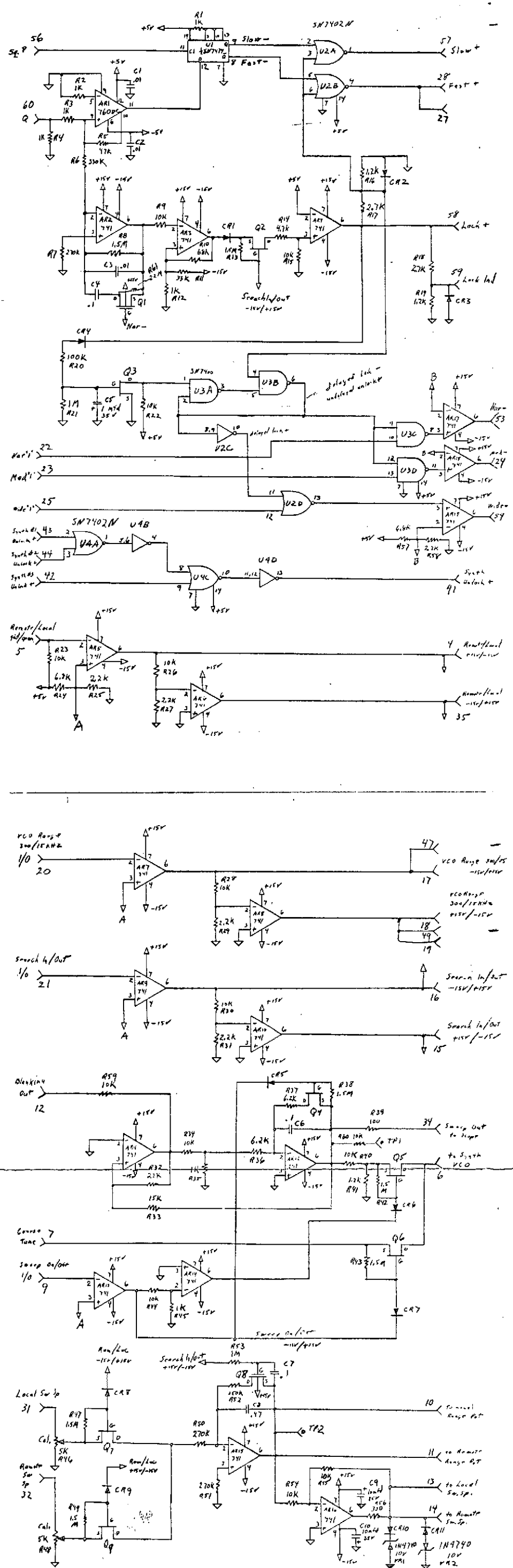


FIGURE 3.2.15A

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REPRODUCIBILITY OF THE
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Control Board

FIGURE 3.2.15B

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3-45

heterodyning the VCXO to 40 MHz in the 15 kHz mode rather than multiplying, heterodyning, and again multiplying (total multiplication x20) to 40 MHz as in the 300 kHz mode. This equalization of gain is necessary to maintain the same tracking bandwidths in the 15 kHz VCXO range mode as in the 300 kHz VCXO range mode.

The bandwidths are as follows:

Wide B_L	1.0 kHz
Medium B_L	100 Hz
Narrow B_L	10 Hz

These bandwidths are referenced to 40 MHz.

The output of AR1 is summed in AR3 with tuning and sweep or decay voltages from AR11. The output of AR3 controls the tuning of the VCXO.

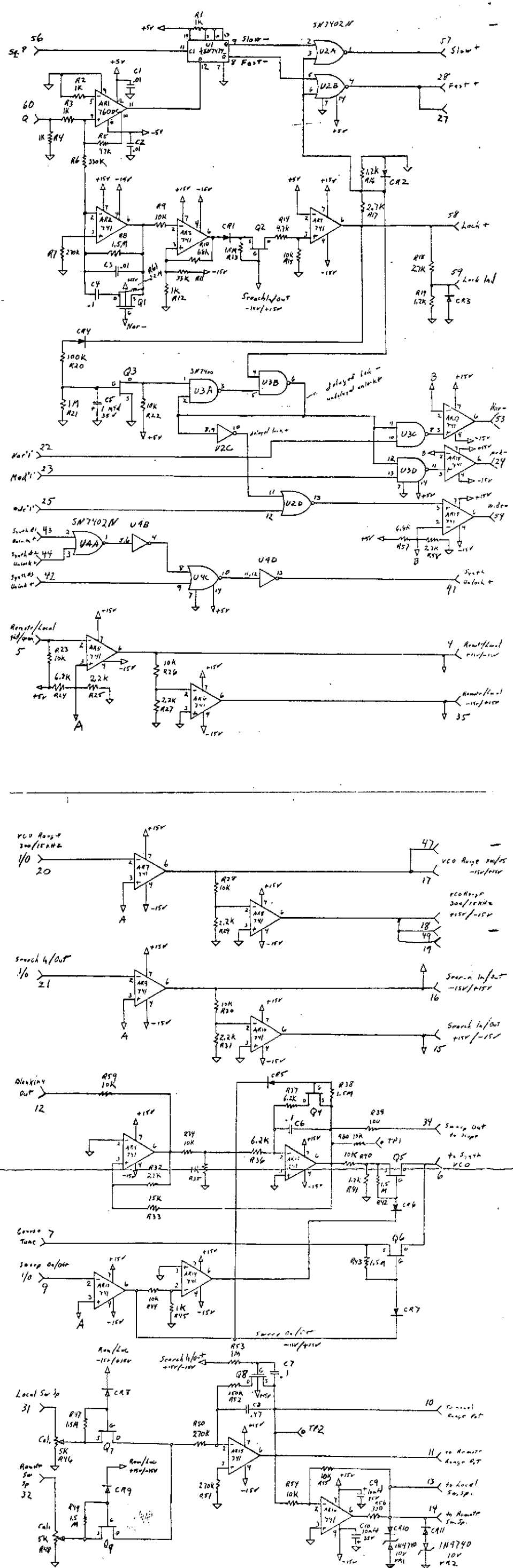
2) Correlation Detector

The correlation detector has been moved to the exciter control board to alleviate crowding on the Loop Filter/Acquisition Board. See Schematic of Figure 3.2.15B.

AR2 and associated components act as an active filter to detect the continued presence of the proper polarity of "Q" detector output. The time constant is switched to a longer time in the narrow loop bandwidth to avoid flickering of the correlation output on low beatnotes before lock.

AR3 is used as a comparator with hysteresis due to positive feedback. When the "Q" input has been sufficiently positive for a time determined by the switchable time constant,

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Control Board

FIGURE 3.2.15B

REPRODUCIBILITY OF THE
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3-45

the output of AR3 goes positive. This condition is disabled by Q2 in the Search IN mode. In the Search OUT mode, the output of AR4 goes positive and is used for various switching functions.

3) The Decay Forcing Function

The "Fast" and "Slow" detector circuits which determine that the VCXO frequency is too high or too low have also been moved to the Exciter Control Board.

Squared "P" and "Q" signals are applied to the Clock and Data inputs of U1, a D type FF. If "Q" on the data input goes positive before the "P" clock goes positive, the "Fast -" signal goes to a logic zero. This indicates that the VCXO frequency is too high. If the "P" and "Q" signals arrive in the opposite order, the "Slow -" output goes to logic zero, indicating that the VCXO frequency is too low.

Both signals are gated with the Lock "+" in OR gates to hold both outputs at logic zero during lock. The inversion in the gates results in "Slow +" or "Fast +" signals when the correlation circuits do not indicate lock.

Lamp drivers elsewhere in the system drive panel lamps for the Fast and Slow arrows.

The "Slow +" signal is sent to the Loop Filter/Acquisition Board for use in deriving the Decay Function which returns the VCXO to center frequency automatically in the "acquire" mode.

Other housekeeping functions are also on the Exciter Control Board.

The Fast + signal drives the output of AR6 of

the Loop Filter/Acquisition Board negative.

This is limited by a resistor and zener diode combination to about 6.1 volts. This signal is disabled by Q8 in the Search IN mode or after lock has been acquired. In the Search OUT mode, until lock, this signal is the basic decay forcing function, modified in size by switches Q9 and Q10 according to the truth table below. This function is of the proper polarity to drive the VCXO to the correct frequency to lock to the standard. Note that if the "Fast +" signal had gone to logic zero, the polarity of the forcing function would reverse. E is the size of the forcing function.

VCXO RANGE	300 kHz			15 kHz		
	Q11	Q12	Evolts	Q11	Q12	Evolts
Fast Decay	Closed	Open	.66	Open	Open	6.1
Slow Decay	Closed	Closed	.06	Closed	Open	.66

Decay Slow-Down - The square wave "P" from AR4 is also applied to U1, an SN74123N retriggerable multi-vibrator. As long as the beat note retriggers U1 often enough, \bar{Q} remains negative. At lower rates \bar{Q} goes positive between cycles and clocks U2. The time constant is switched by Q6 and Q7 depending on loop bandwidth. As the VCXO approaches the correct frequency, the beat note will be fast enough to prevent clocking U2 until the beat note drops to the frequencies listed.

	referred to 40 MHz	referred to S-Band
Wide BW	1350 Hz	5400 Hz
Medium BW	310 Hz	1240 Hz
Narrow BW	150 Hz	600 Hz

Search IN resets U2 so that \bar{Q} is positive until clocked. The output of AR5 is negative until U2 is clocked. When it is time to slow down the decay ramp, U2 is clocked, AR5 output goes positive, and appropriate switching occurs. The decay ramp slows down by about a factor of 10 in time to acquire.

"Corner" transients at the start of the decay when switch Q8 closes or when Q9 or Q10 cause slow-down would cause the 3rd order loop in the receiver to lose lock. For this reason AR8 performs an integration so that the decay function rises or falls to a new level slowly. When the output of AR8 reaches the decay value at the input of AR7 it will halt until the decay function is changed in level by AR6, Q8, Q9 or Q10. It will then ramp slowly to the new value. The slope of this ramp is switched to appropriate values for the three exciter tracking bandwidths by Q11 and Q13, which add capacitors C6 and C7 to the time constant. Q12 and Q14 keep C6 and C7 discharged when not in use.

The decay ramp generating voltages tabulated are arranged to increase the ramp slope X10 when in the 15 kHz VCXO range mode. This nearly compensates for the X20 loss in transmitter frequency response to VCXO ramps. For this reason it is not deemed necessary to switch the slowdown time constant of U1 for different VCXO ranges. The output of AR8 will be applied to AR9 through 4.7 megohms to be integrated by AR9 into the ultimate decay ramp with no "corners". To determine the optimum values for C5, C6 and C7 it will be necessary to have a complete simulated round-trip system with

a transponder simulator and receiver with third order loop. Other portions of the acquisition circuitry can also benefit from complete system tests.

AR9 sums the decay ramp with the VCXO tuning and sweep described below.

4) Tuning and Sweep

The Local Tuning and Local Sweep come in on separate wires and are summed together with feedback at the source of Q20. Switch Q20 disables these signals in the Search OUT mode or in the "Remote" mode. There is a time delay in removing these signals so that Q16 and Q18 may complete their function of switching ramp time constant before Q20 opens. These three signals are all switched by the same transistor because the feedback must be removed at precisely the same time as the tuning and sweep to avoid a transient.

Remote Tuning and Remote Sweep are summed with their feedback resistor at the source of Q21. Switch Q21 disables after a similar time delay on Search OUT or in the Local Mode.

Both tuning pots are precision 10 turn film potentiometers capable of resolving 10 Hz out of 300 kHz. They will be supplied with 1000 division, 10 turn logging dials which can be trimmed so that center frequency reads 500. Zener diodes to reduce +15 volts to ± 8.2 volts will be mounted on the acquisition board in order to establish a more effective common ground with the rest of the acquisition circuitry.

Both Local and Remote Sweep Range pots will be clockwise A taper (modified logarithmic). This will result in

a usable calibration at low values of sweep range. A calibration trimmer will be provided at each control panel.

The Local and Remote Sweep Speed pots will be linear and arranged to give a calibration essentially linear from 1 to 20 seconds.

5) Summation of Decay, Sweep, and Tuning

As described in previous paragraphs, tuning, sweep and feedback are supplied by Q20 or Q21 in the Search IN mode. A decay forcing function is supplied from AR8 circuitry in the Search OUT mode. These signals are applied to the summing point of AR9.

In the Search IN mode a .047 μ F capacitor causes AR9 to integrate quite rapidly. It is fast enough that the Manual Tuning does not feel "sloppy", yet slow enough to slightly round the corners of the triangular search sweep. This latter helps a third order loop in the receiver to avoid breaking lock at the corners.

In the wide bandwidth the same .047 capacitor integrates the decay forcing function into a ramp back to the correct center tuning.

In the medium bandwidth an additional .68 capacitor is added if the exciter is switched to Search OUT. In the narrow bandwidth a 10 mfd capacitor is added if the exciter is switched to Search OUT. These capacitors are kept discharged by Q19 and Q17 until switched into the circuit by Q18 and Q16. The latter are slightly delayed in order that the Q19 or Q17 grounds can be removed before Q18 or Q16 close. This avoids a serious transient.

The result of the above paragraphs is to slow down the decay ramp by a factor of 16 in the medium bandwidth and by a factor of 160 in the narrow bandwidth.

The essentials of this system have been used and tested. Improvements in the decay ramp shape, and more switching, should result in improved speed over the table below. This table represents test values on an existing equipment. See Section 4.4 for computed values of time-to-lock expected from the latest design.

	Wide	Medium	Narrow
Exciter B _L referred to 40 MHz	1.0 kHz	100 Hz	10 Hz
Use with receiver BW	1 K - 3 kHz	100 - 300 Hz	10 - 30 Hz
<hr/>			
±300 kHz VCXO Range			
<hr/>			
Decay forcing volts, fast	.66	.66	.66
ditto after slowdown	.06	.06	.06
Decay rate at S-Band, fast	29.2 kHz/sec	29.2 kHz/sec	641 Hz/sec
ditto after slowdown	2.65kHz/sec	2.65kHz/sec	58 Hz/sec
Beatnote at Slowdown	44 kHz	44 kHz	3 kHz
Approx. time to lock from 300 kHz	19 sec	19 sec	500 sec
<hr/>			
±15 kHz VCXO Range			
<hr/>			
Decay forcing volts, fast	not used*	not used*	6.1
ditto after slowdown	.66	.66	.66
Decay rate at S-Band	not used*	not used*	297 Hz/sec
ditto after slowdown	1.46 kHz/sec	1.46 kHz/sec	32 Hz/sec
Beatnote at slowdown	44 kHz*	44 kHz*	3 kHz
Approx. time to lock from 15 kHz	13 sec	13 sec	50 sec

* Note that starting at ±15 kHz one is already in the slow decay zone because less than 44 kHz beatnote causes slowdown.

6) Sweep Generator

The sweep generator has also been moved to the Exciter Control board. Switches Q7 and Q9 provide for a choice of local or remote control of sweep time. Separate trim for each local and remote at 20 seconds is provided on the control panels. Separate calibration at 1 second is provided on the control board. These two trim controls will permit exact calibration at 2 seconds and at 19 seconds, with 1 second and 20 seconds being in some doubt because of the less accurate control of the curve at the end of the potentiometer.

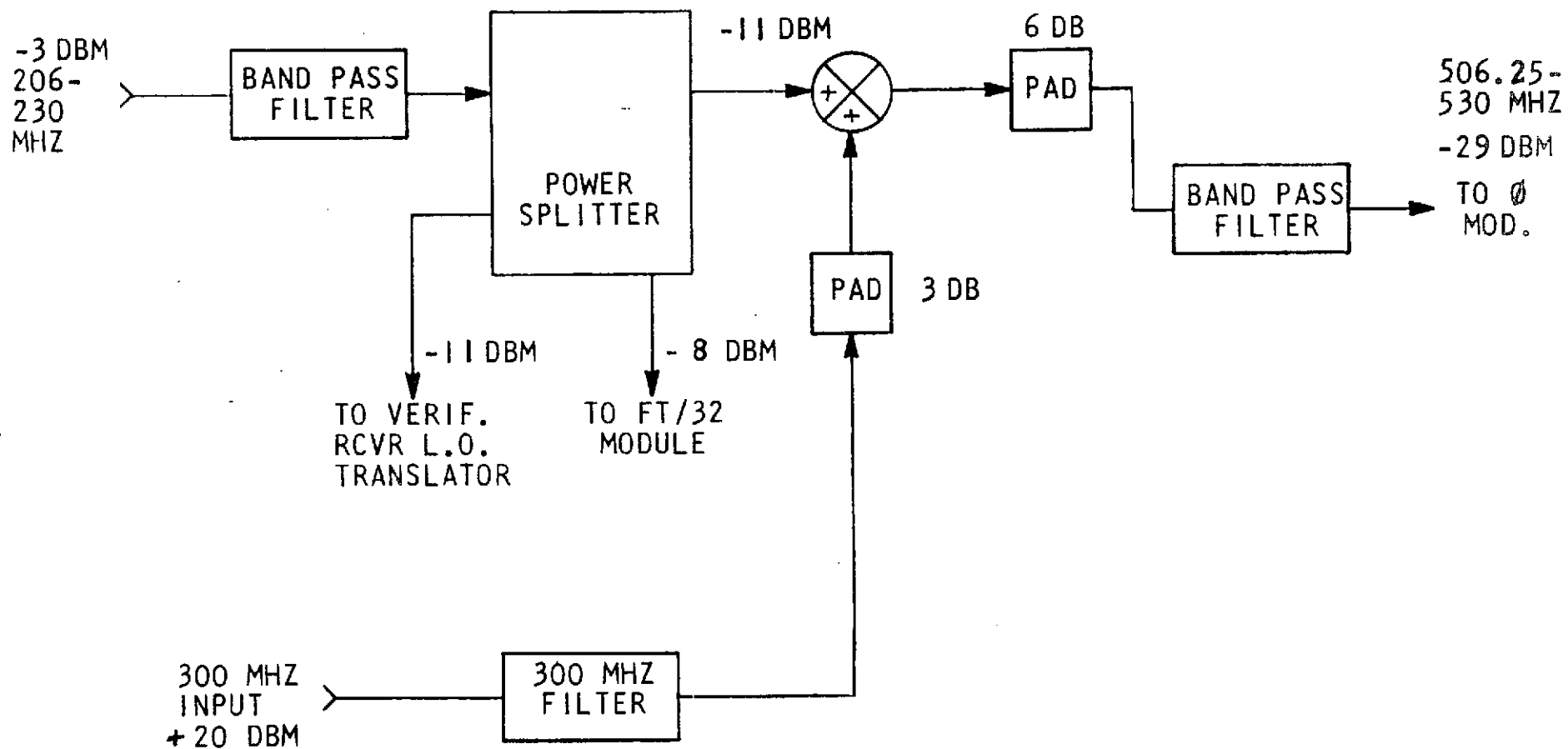
Range pots are provided on the two control panels with individual trim pots. The range pots will be modified logarithmic (taper A) as described previously to make the calibration useful at low sweep amplitude.

3.2.6 Up Converter

The function of the up converter is to mix the two final signals used in generating the transmitter signal before it is multiplied times 4. This circuitry will be chassis mounted as shown in Figure 3.2.16 .

The 300 MHz L.O. signal, as selected in the FM module, is fed into the mixer through a 3-pole bandpass filter used to eliminate harmonics of the input frequency and a 3 dB pad. The level which is variable at the FM module is maximally at a level of +20 dBm and incurs a 2 dB loss through the filter as well as the 3 dB from the fixed pad. The L.O. operating levels of the High Level Olektron Corporation O-CHD-146 will be variable from +10 dBm to +15 dBm and will be set for optimum spurious response. The 3-pole filter is used to further reduce the components of the 125 MHz and 175 MHz mix as well as 150 MHz components of the doubler in the FM module when the 300 MHz is generated. The passband of the filter is 16 MHz, and while insuring all components aforementioned to be greater than 90 dB below the desired, will provide adequate bandwidth for preserving FM fidelity and minimize delay.

The linear input from 206 to 230 MHz comes into the module at a level of -3 dBm and is filtered as it is fed into a 3-way power divider made up of two 1715 Hybrid dividers. After a 2 dB loss in the filter, the input at -5 dBm is split into two paths at a level of -11 dBm and one at -8 dBm. Two paths are to other modules as shown in Figure 3.2.16. The other output of the divider is the linear input to the mixer. Using the excellent characteristics of the high level mixer



UP CONVERTER
FIGURE 3.2.16

and controlling the input levels will warrant the inband spurious 12th order $(6 \times R) - (6 \times L)$, 5th order $(4 \times R) - (L)$ to be down greater than 85 dB from the desired output of 506 to 530 MHz.

The output from the mixer is padded by 6 dB to a level of -18 dBm and filtered by a 6-pole bandpass filter before being injected into the phase modulator. The filter characteristics must be sufficient to insure a signal that is spurious free to at least 72 dB from the desired. The close band spurious will be a $(3L) - 2(R)$ which would be at 488 MHz when the desired frequency is at 506 MHz. For a high level mixer such as the ZAD-1WH, and a -10 dBm input, this frequency should be 75 dB down out of the mixer. The input levels to the mixer must be adjusted to obtain this condition since the filter 3 dB bandwidth will extend to 488 MHz and thus provide no rejection to this signal.

3.2.7 FM Generator

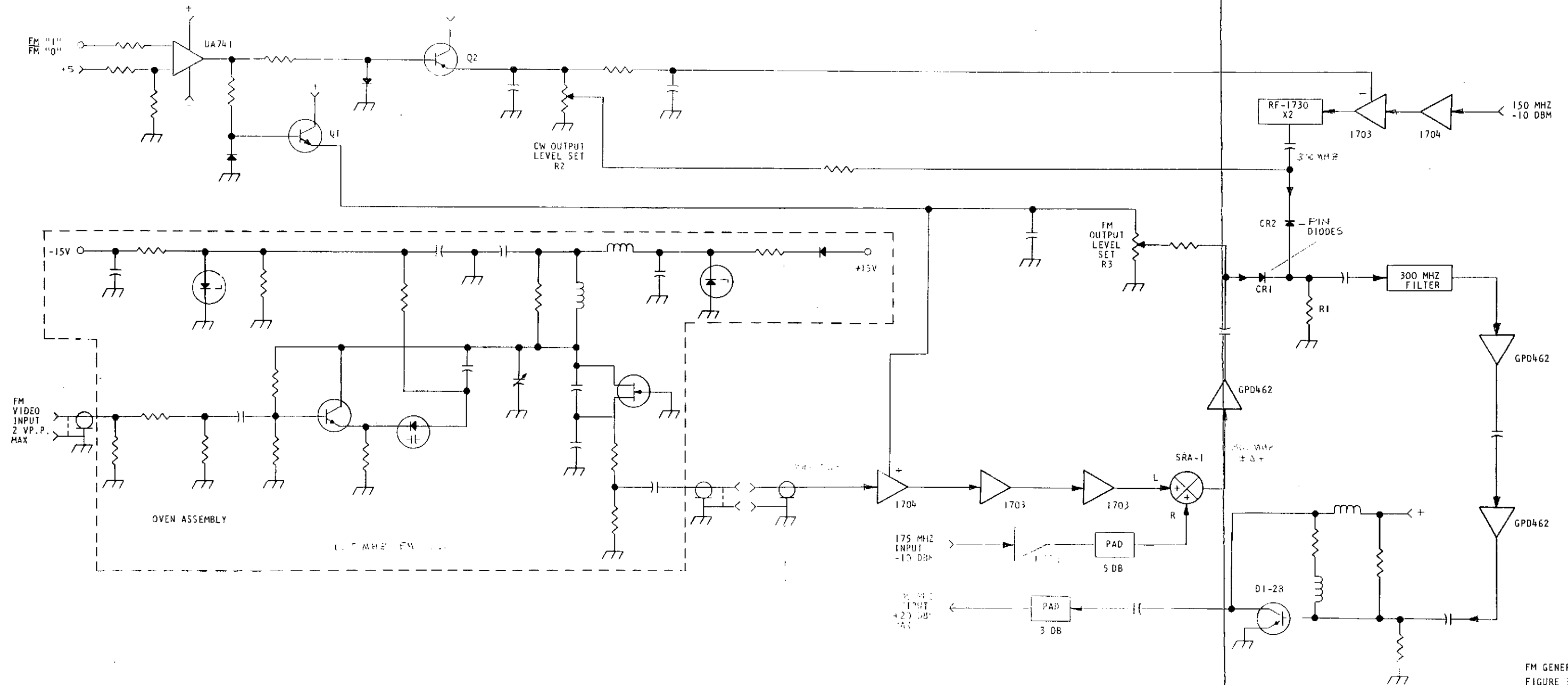
The FM generator module contains the modulated VCO used to generate the FM for the system and also a frequency translator which develops either an FM 300 MHz signal or a 300 MHz CW signal to be used in the up converter. Refer to Figure 3.2.17 for the block diagram of the FM module.

The 300 MHz is generated by doubling a 150 MHz CW signal in one instance and by an additive mix of the 125 MHz VCO signal with a 175 MHz signal. In either case the selection is aided by switching off the undesired signal. The switching action is initiated by a logic level signal into the $\mu A741$ operational amplifier which is run at full open loop gain to act as a threshold latching switch. The threshold of this switch is set by a voltage divider which is set at $1/2$ the level of a logic "1". Since the input is to the non-inverting input, the amplifier will latch to B+ for a "1" input and B- for a "0". For a "1" input, Q₁ will be turned on switching on the VCO and forward biasing CR1. When the "0" input is programmed, CR2 and the RF-1703 amplifier tied to Q₂ will be on.

In the $\overline{\text{FM}}$ position, ("0"), the 150 MHz input is amplified in an RF-1704 amplifier and fed to the RF-1703 which is switched on. This output is raised to a level of +11 dBm and drives the balanced doubler RF-1730. The doubler output passes through the switch CR2 to resistor R1. The output is set to a nominal -5 dBm to be compatible with the 300 MHz FM signal. The level is controlled by variable resistor R2 which controls the impedance of CR2 by varying the forward bias.

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FM GENERATION
FIGURE 3.2.17
3-55

FOLDOUT FRAME 1

FOLDOUT FRAME 2

From resistor R1, the signal is coupled to a 2-pole bandpass filter to remove some of the undesired doubler and mixer products prior to amplifying the desired level to +20 dBm. This filter is minimal to aid only in reducing cross modulation by components not cancelled sufficiently in the doubler and mixer. A coaxial filter external to the module is employed before the 300 MHz is used as a mixer input.

The level from the filter is amplified from -10 dBm to +23 dBm with two Avantek amplifiers, GPD462 and GPD463, and a CTC transistor stage D1-28Z. The output is padded 3 dB before leaving the module. This pad will aid in furnishing a 50 ohm driving impedance while loading the output stage to provide a margin of stability.

When FM is chosen ("1") at the input to the operational amplifier, Q1 switches on and Q2 switches off which reduces the input to the passive doubler by turning off the RF-1703 amplifier. Since the doubler must have sufficient voltage to turn the diodes on, the output will drop to zero. Any other leakage that should come through will be further attenuated by reversed biased diode CR2.

Turning Q1 on furnishes the B+ to the 1704 Amplifier shown in Figure 3.2.17. The frequency modulator is an oven enclosed VCO using a FET for the oscillator. Although the FET oscillator draws very little power which could contribute to a period of stabilization during warmup, the oscillator is

kept on continuously in the oven environment so as to be used immediately at its ultimate stability. Tests of the breadboard model in the environmental chamber at 65°C show the nominal frequency deviations to be within ± 2 kHz at this stabilized temperature.

The conventional Colpits type oscillator is frequency modulated by varying the capacitance of a hyper-abrupt varactor diode which is fed from the low impedance point of an emitter follower. With a multiplication factor of 4, only 250 kHz deviation is necessary for the oscillator. Breadboard tests of this circuit have shown that this can be accomplished with rates exceeding 5 MHz without difficulty. Using a wide band discriminator (4 MHz between peaks of the "S" curve) for an FM detector, an IM test on the FM generator showed all cross products to be down at least 45 dB from the detected modulating frequencies.

This particular VCO design was selected after deficiencies of an earlier proposed design surfaced. An earlier proposed VCO design called out in the Preliminary Design Evaluation Report, S-Band Exciters, Contract No. NAS5-20464, was found to exhibit a frequency jump of the center frequency. This phenomenon was attributed to frequency modulation from both the varactor diode in the emitter path and the variation of collector capacitance of the same transistor. Tests showed that replacement of the varactor diode by a fixed capacitor only reduced the frequency deviation of the VCO and did not eliminate it. This frequency excursion of the carrier was found to be 20 kHz as displayed on a spectrum analyzer at a

VCO frequency of 125 MHz. The later design does not exhibit this undesirable characteristic.

The 125 MHz output from the VCO is modulated with the FM video input that is switched in from the Phase Modulator module. The modulated output is amplified by buffer amplifiers to a level of +8 dBm and used as the local oscillator injection into the Minicircuits Laboratory SRA-1 mixer. The linear input to the mixer is 175 MHz which enters the module at -10 dBm, is amplified and padded back to -10 dBm. This action presents a 50 ohm impedance to the mixer and provides isolation to the other modules.

The output of the mixer at 300 MHz will be at a level of -18 dBm. No serious spurious will be present for this narrow band mix. The signal is amplified in an Avantek GPD462 amplifier to a level of -5 dBm and passed through forward biased diode CR1 to resistor R1. The level at R1 is controlled by varying the forward bias of CR1 by variable resistor R3. This adjustment, which is identical to that described for CR2, allows setting the CW and FM levels at R1 to exact levels. The path from this point is identical to that discussed for the doubled 150 MHz signal.

3.2.8 Phase Modulator/Modulation Input Circuits

The function of this module is to select the proper modulation, provide an analog signal for metering the selection and phase modulate or PSK modulate the input r-f signal. The operation of this module is discussed with reference to Figure 3.2.18 which indicates the various operating levels.

The circuitry involved in this module is for the most part generally routine except for the wide band phase modulator comprised of a 3 dB quadrature hybrid and varactor diodes.

The operation of the quadrature hybrid for equally loaded output ports (not necessarily Z_0) is such that the reflected power for a non Z_0 termination will split between the input port 1 and the isolated port 4. (The power absorbed by the terminated reactances will be negligible due to the high Q voltage variable capacitors). The phase relationships of the reflected power is such that the reflected power at port 1 from the mismatched ports 2 and 3 will be out of phase and cancel, yielding a low input VSWR. The reflected power at port 4 will be in phase and additive. Varying the phase between the input and output using this principle is the basis for the phase modulator. The phase is changed by varying the voltage varying the reactance of the hyperabrupt junction diodes at ports 2 and 3.

The varactor diodes used in this phase modulator are Motorola MV3140s. These diodes possess a very linear voltage vs capacitance relationship over a wide range. Their characteristics are such that any particular batch of diodes from the same production run are very closely matched thereby simplifying

FOLDOUT FRAME /



3-60

alignment of the phase modulator for linearity.

Selection of the hybrid is important in that unbalanced loading of the output ports can detract from the linearity and can be caused by the hybrid itself not being equally balanced. This can be remedied to some degree with tuning for small bandwidths. Incidental AM could also result from this condition but would be eliminated by the limiting action of the X4 multiplier.

The phase modulator is driven by the transistor amplifier Q₁ and Q₂ which inverts the signal in Q₁ to give a positive modulation polarity and is driven by the low impedance of emitter follower Q₂. The input modulation levels of 0 to 4 volts peak to peak is sufficient to produce the 0.75 radians peak, however Q₁ will furnish an additional gain of 2 to insure a safety factor and still not degrade the system noise in the modulation path. A bias adjustment pot is located in the emitter of Q₁ to set the reverse bias of the varactor diodes at +5 volts. A similar type phase modulator used in NASA's S-Band Transponder Simulator, under NAS5-20396, has a sensitivity of 0.25 radian peak/volt p-p which would give the desired .75 radian peak for 3 volts p-p before the X4 multiplication which yields the desired 3 radians peak.

The r-f path for the phase modulator is through two Avantek GPD462 amplifiers which furnish a minimum gain of 26 dB. From an input level of -26 dBm, the input signal to the quadrature hybrid is 0 dBm. The loss through the hybrid is a maximum of 4 dB which brings the modulated signal at the output of the hybrid to a level of -4 dBm. This output is

padded by 3 dB and amplified to +15 dBm by Avantek GPD462 and D 128 amplifiers. This output is fed to the X4 multiplier in the antenna electronics assembly.

Selection of the modulation is performed with FET switches which are activated by μ A741 operational amplifiers which are associated with the switches as shown in the diagram. The μ A741s are biased to a level such as +2.5 volts. When the non-inverting input to them is 0 or less than +2.5, the amplifier output is negative shutting off the FETs or providing a high impedance. When a 1 or $>+2.5$ volts is applied to the input, the FET is switched on and provides a low impedance across the device.

All three inputs (FM, PM, and PSK) arrive on the same cable which is terminated in 51 ohms. Selection of the proper modulation is described in the paragraph above. When FM is selected, the modulation is switched into the LH0002CN line driver which sends it out of the module to the FM module. When PM is selected it is sent to Q1, Q2 and the Anaren Quadrature hybrid as described above. When the PSK is switched on, the signal is limited so that when it is applied to the linear PM modulator the phase shift will be held at $\pm 22.5^\circ$ ($\pm 90^\circ$ at S-Band). The incoming PSK signal will be at logic levels.

Note that the PSK RF at S-Band will change from -90° to $+90^\circ$ or reverse by passing through 0° at full amplitude. It will not drop to zero amplitude by going directly from -90° to $+90^\circ$. This distinction will become important when the PSK demodulator is discussed under the Verification Receiver heading.

Whichever type of modulation is used, the incoming video will be sent to the peak detector circuits to operate the Modulation Meter. In the FM mode, the meter amplifier, AR3, has less gain due to Q6 shunting the feedback resistor with a smaller value. Full input of 4 volts peak-to-peak will read slightly over 1.00 volts. The gain of the FM modulator circuits will be set by means of R3 so that 1.00 volts indicates 1.0 MHz deviation.

In the PM mode the meter amplifier, AR3, will have a higher gain so that 4 volts peak-to-peak will read a little over 3.00 volts. The PM gain will be adjusted by means of R2 so that 3.00 volts indicates 3.0 radians PM.

In the PSK mode the meter sensitivity will be the same as for PM. If 4 volts peak-to-peak arrive at the input, the meter will read a little over 3.0. This will indicate adequate input, but will not mean 3 plus radians. The limiter and R1 will be set to give $\pm 90^\circ$ at S-Band for any reasonable value of peak-to-peak input.

3.2.9 $f_T/32$ Doppler Output

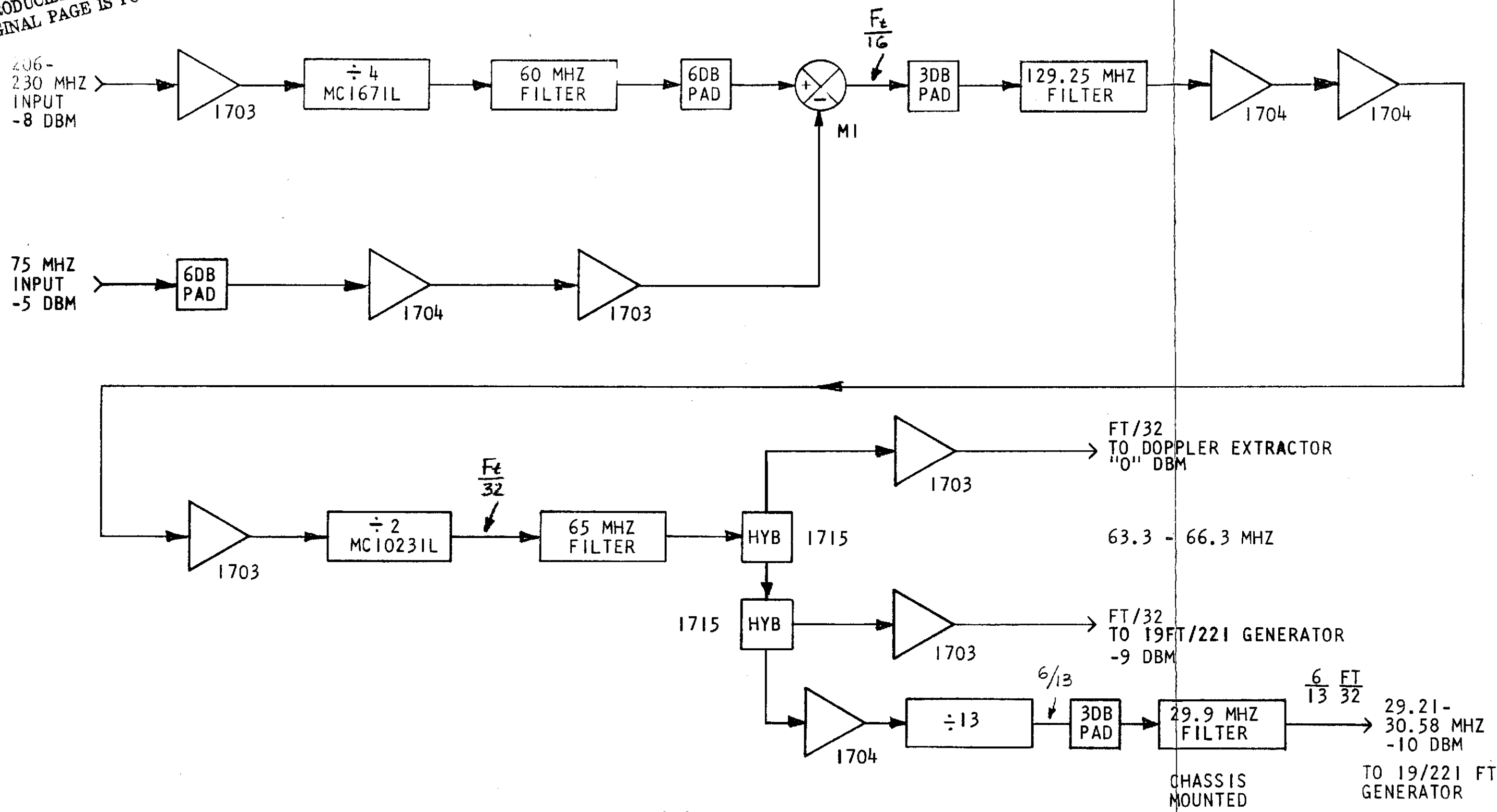
The $f_T/32$ frequency is derived as shown in Figure 3.2.19. A mixer L.O. input at 75 MHz is padded, amplified from a -5 dBm level to +10 dBm with RF-1704 and RF-1703 amplifiers, and injected into a Minicircuits Laboratory high level mixer.

The linear input to the mixer ranges in frequency from 206 to 230 MHz at a level of -7 dBm. This input is amplified to a level of +4 dBm and fed to a +4 chain consisting of two MC1671L dividers. The divided output, a symmetrical square wave, is filtered by a 7-pole low pass filter. Since even harmonics will be suppressed in the square wave output, the third harmonic will be the highest undesirable. Using an elliptic filter design with a ripple of 0.18 dB, the third harmonic will be suppressed 80 dB and any second harmonic present will be reduced by 60 dB.

The input to the mixer will be reduced to -15 dBm to improve spurious response that is present in band. The output of mixer M1 is padded by 3 dB and filtered by a band pass filter as shown in Figure 3.2.19. The following crossover spurs and their attenuation are present as follows: (6L - 6R) and (8R - 4L) > 90 dB, (4R - L) 90 dB, (4L - 3R) 90 dB, (5R - 2L) 90 dB, (7L - 7R) and (9R - 5L) 90 dB.

The closest near band spurious is the fifth order (3L - 2R) which moves in to 122 MHz at the low end of the band. This mixer product will be down 75 dB. The products under discussion must be maintained at these levels since the filter will not aid in reducing them. The high level mixer approach is thus necessary for this particular mix for a 75 dB

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FT/32 GENERATOR
FIGURE 3.2.19

FOLDOUT FRAME

FOLDOUT FRAME

spur free signal to be available to the $19/221 f_T$ generator.

The output of the filter is followed by three stages of amplification which is used to drive a +2 circuit comprised of an MC1023LIL stage. This symmetrical divider is followed by a 7-pole low pass elliptical filter which suppresses the odd harmonics by 80 dB. This filtered signal is $f_T/32$ and is hybrid split and buffered for further isolation into two paths which are directed to the Doppler Extractor module and a second Hybrid Splitter. One output from the hybrid is directed to the Frequency Translator as a $f_T/32$ input.

The second output from the hybrid is amplified and drives a synchronous +13 divider comprised of MC1027 J-K flip flops and MC1023 gates. The 6/13 harmonic is taken from the divider at its most enhanced point and passed through a band-pass filter to remove all 1/13 harmonics with respect to the 6/13 by at least 78 dB. This is essential to meet the 60 dB spurious requirement after a multiplication of 8. A breadboard examination of the spectral distribution revealed the 7/13 harmonic to be only 1 dB down from the desired 6/13 harmonic. The filter required must provide rejection of this component by 77 dB as a minimum. A 5-pole bandpass filter with a center frequency of 29.9 MHz and a 3 dB bandwidth of 1.6 MHz and 0.1 dB ripple will meet this requirement. A maximum insertion loss of 3 dB can be expected from this filter. This output is then directed to the $19/221 f_T$ module.

3.2.10 19 $f_T/221$ Generation

The 19 $f_T/221$ frequency is developed by dividing and mixing the $f_T/32$ signal with the 6/13 $f_T/32$ signal and multiplying the difference frequency as shown in Figure 3.2.20.

The 6/13 $f_T/32$ signal enters the module at a level of -10 dBm. This signal is amplified to a level of +13 dBm and passed through a low pass filter to become the L.O. signal to the mixer which is a high level Minicircuits Laboratory SRA-1-WH mixer.

The linear input to the mixer is derived from the $f_T/32$ input which comes into the module at a level of "0" dBm. This signal is buffered in an amplifier and fed to a +17 synchronous divider. The 2/17 harmonic is selected at its most enhanced point in the divider network. Measurements of the +17 spectrum was made and the fundamental and third harmonic was shown to be 17 dB and 19 dB down from the 2/17. The filter following the divider is then required to provide a minimum of 61 dB rejection of these harmonics. A 3-pole bandpass filter with a 3 dB bandwidth of 1 MHz and .01 dB ripple will yield the desired results.

Output from the bandpass filter is padded to become the linear input to the mixer. Using the high level mixer and adjusting the variable input will optimize in-band spurious responses which can be anticipated as follows:

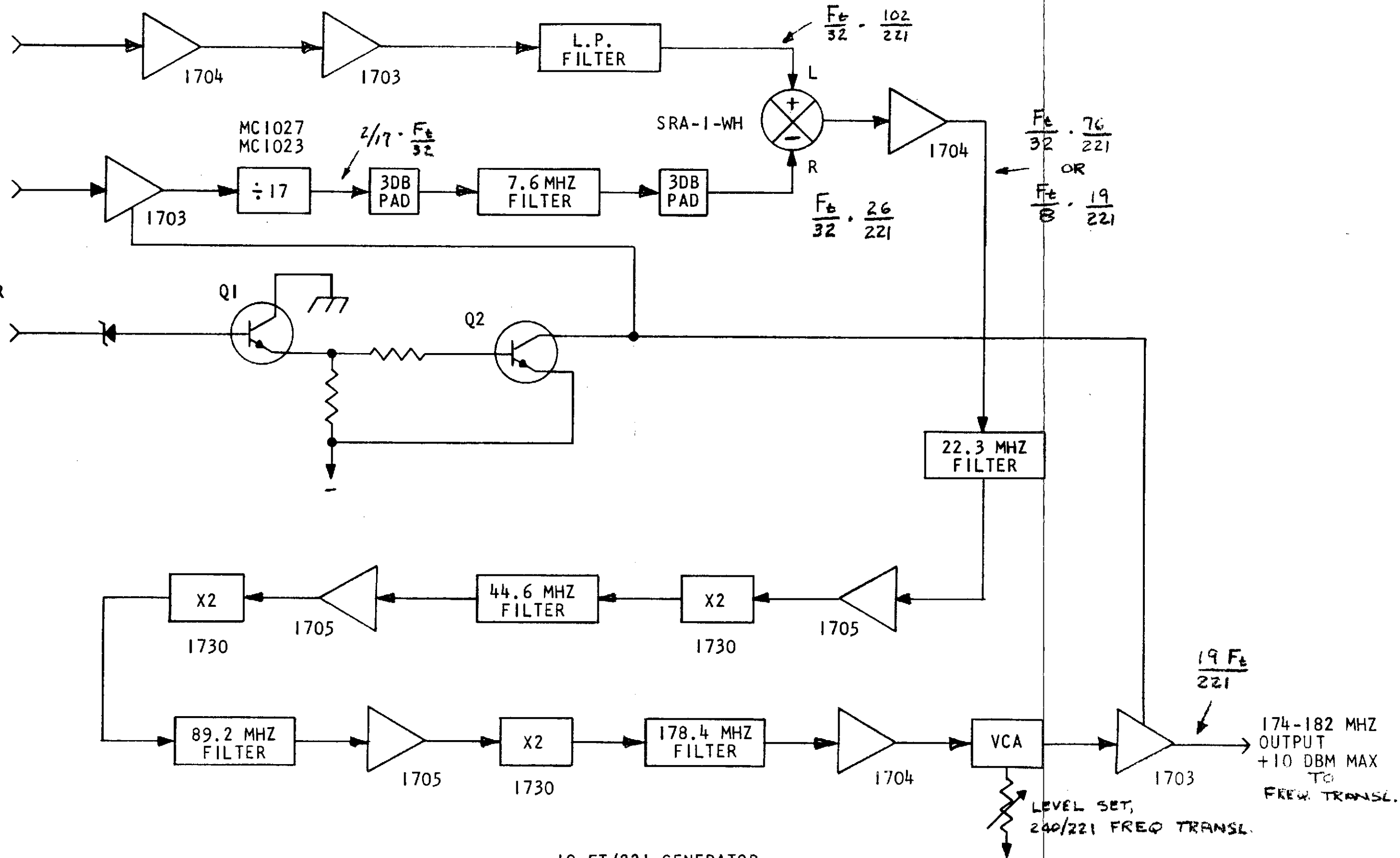
3A, -87 dB, 2B - 5A, -87 dB, and 7A - B, -90 dB
where A is 2/17 x $f_T/32$ at a nominal level of -10 dBm and B is 6/13 $f_T/32$ at a level of +13 dBm.

The subtractive mix is amplified and passed through

$\frac{6}{13} \frac{F_t}{32}$
 29.21-
 30.58 MHz
 -10 DBM

FT/32
 63.3-
 66.3 MHz
 0 DBM

TRANSLATOR
 ON/OFF
 CONTROL
 "1" ON
 "0" OFF



19 FT/221 GENERATOR
 FIGURE 3.2.20

FOLDOUT FRAME 1

FOLDOUT FRAME 2
 3-68

a bandpass filter with a 1.8 MHz bandwidth. The closest out of band spurious will be the L.O. feedthrough which will be 35 dB down out of the mixer and rejected another 50 dB by the filter.

The output from the mixer filter at a level of -9 dBm is amplified to +7 dBm and multiplied by 2 in a balanced doubler. Suppression of the fundamental and third harmonics of the input is greater than 30 dB at this frequency. The 2-pole bandpass filter which follows the doubler has a 3 dB bandwidth of 4 MHz and further rejects the fundamental and third harmonic by 40 dB.

The signal is again amplified and doubled to a center frequency of 89.2 MHz and passed through a 2-pole filter with a 3 dB bandwidth of 7 MHz. This filter along with the odd harmonic suppression of the doubler will bring the first and third harmonic down 62 dB from the desired. Further rejection to these frequencies will be performed in the next filter.

The output at the 89.2 MHz center frequency is amplified and doubled for the desired output frequency. The doubled output is filtered by a 2-pole filter with a 3 dB bandwidth of 12 MHz. This filter rejects the closest harmonics of 89.2 MHz by 72 dB and the doubler offers an additional cancellation of 10 to 20 dB.

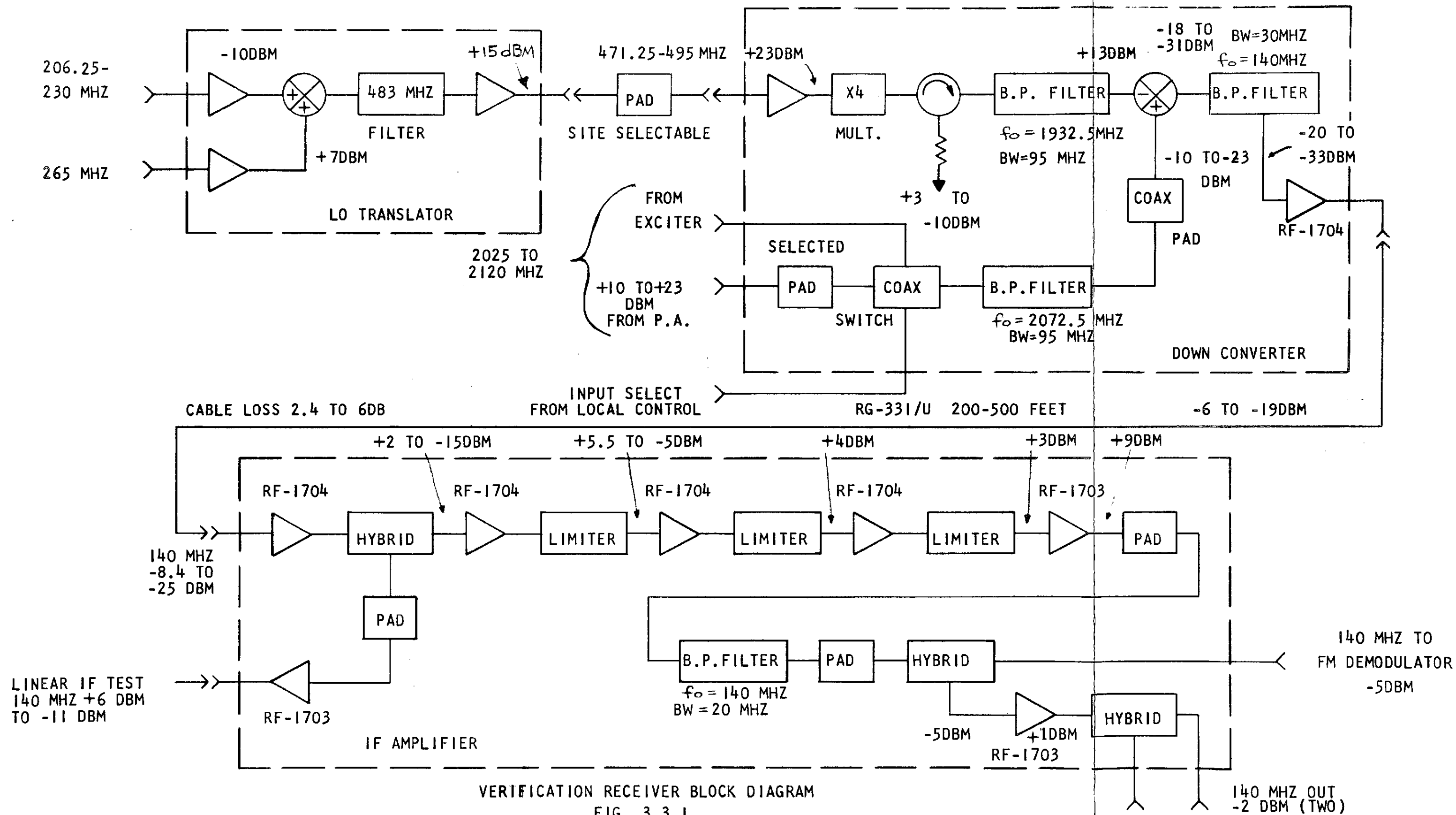
The filtered output is amplified to a maximum level of +10 dBm. The output level is controlled over a 10 dB range by a voltage controlled attenuator which is used to set the desired output for interface with the Frequency Translator which will be located up to 700 feet away.

When the translator is to be turned off, a "0" on the cathode of zener diode CR1 will cause the diode to cease conducting since the breakdown voltage will be insufficient. Q₁ will then turn off and cause Q₂ to turn off which will turn off the amplifier driving the +17 divider and the final output amplifier. The reverse is true when the translator is to be turned on and a 1 or + voltage appears on the cathode of CR1.

3.3 Verification Receiver

The Verification Receiver is a single conversion receiver tuned by the exciter which is used to recover PM, FM or PSK modulation on the up-link signal. The front end of the receiver is located at the antenna and is housed in the same enclosure as the exciter output amplifier (see Section 3.8).

The remainder of the receiver is located in a drawer in the exciter rack. Power to this drawer is supplied from the DC supplies in the exciter control drawer. Figure 3.3.1 is a block diagram showing the down converter and IF amplifier of the Verification Receiver. Selection of the PA or exciter input is made by a coaxial relay which is controlled by a lighted push-button switch on the local test control panel. The "PA" position is the normal or de-energized position for the coaxial relay. See Section 3.8.1.3 for a description of the Verification Receiver Down Converter.



VERIFICATION RECEIVER BLOCK DIAGRAM
FIG. 3.3.1

FOLDOUT FRAME 1

FOLDOUT FRAME 2

3.3.1 L.O. Translator

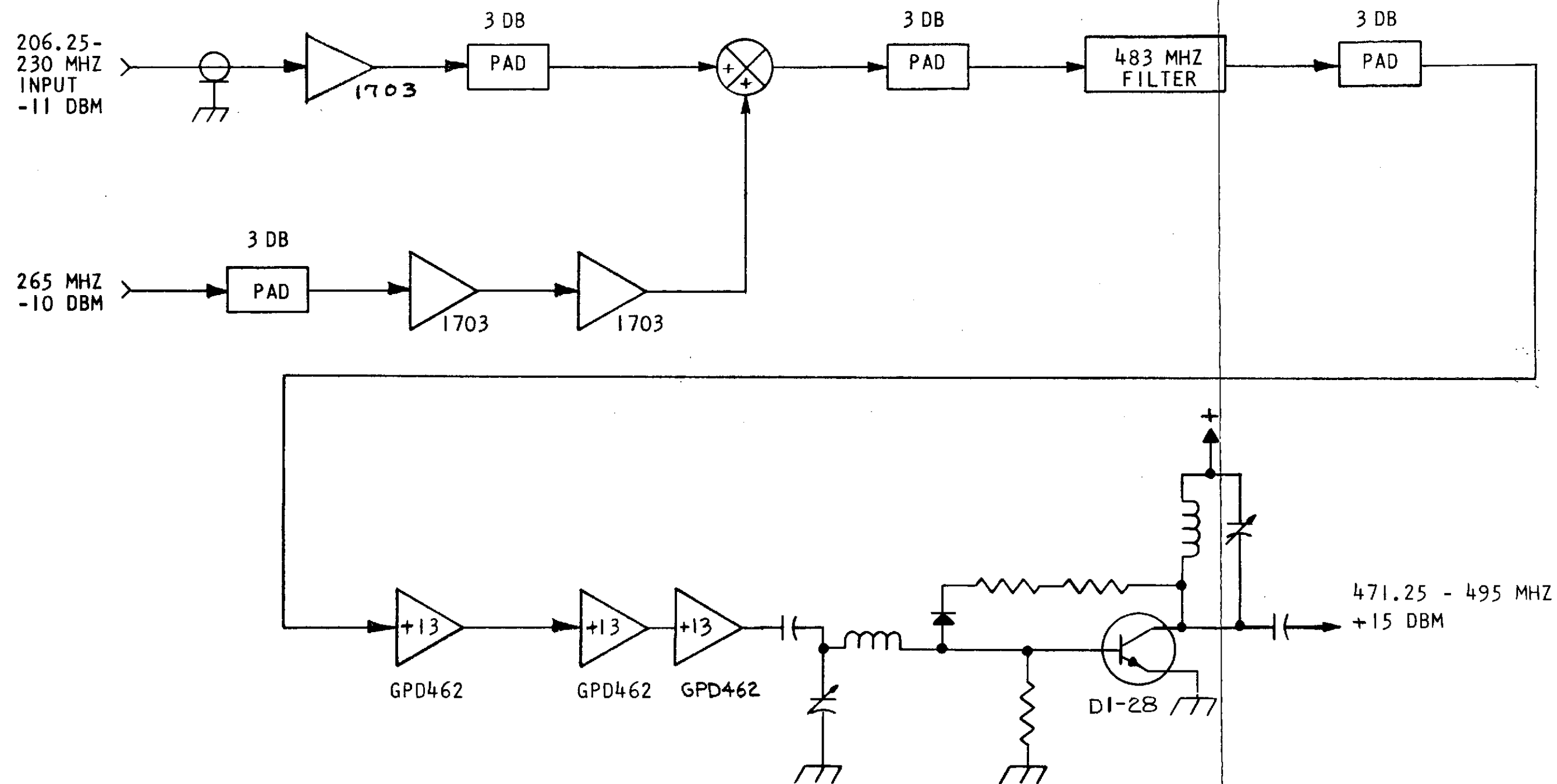
The L.O. translator is shown in Figure 3.3.2. This module translates the band of frequencies 206.25 MHz to 230 MHz to 471 MHz to 495 MHz with an additive mix of 265 MHz.

The 265 MHz enters the module at a level of -10 dBm. It is padded down by 3 dB and amplified to a level of +8 dBm to become the L.O. injection into the double balanced mixer. The linear input which enters the module at a level of -10 is likewise padded down to -13 dBm and fed to the mixer "R" port. The summed output is padded and filtered in a 5-pole bandpass filter with a bandwidth of 30 MHz. The in-band spurious and their levels are:

5L - 4R, 85 dB	6R - 3L, 74 dB
6L - 5R, 90 dB	7R - 4L, 85 dB
7L - 6R, 90 dB	8R - 5L, 90 dB

The closest out of band product is a 4L - 3R which should be down by 77 dB. The second harmonic of the 265 MHz input is at 530 MHz and suppressed by 35 dB by the mixer. The filter will provide an additional 56 dB for a total of 91 dB. The second harmonic of the highest "R" input will be at 460 MHz and should be down by 73 dB. The filter will add another 30 dB of rejection for a total of 103 dB. Good shielding and r-f techniques are employed to meet these goals.

The filtered output is further amplified by a chain of Avantek GPD462 amplifiers and a D128 stage to raise the output to a level of +15 dBm.



L.O. TRANSLATOR

FIGURE 3.3.2

3.3.2 IF Amplifier

The 140 MHz input level to the IF amplifier module ranges from -8.4 dBm to -25 dBm for a 13 dB input signal range at the down-converter and a 3.4 dB range due to differences in cable length (200 to 500 feet of RG-331) from site to site. The limiter system has a range in excess of 35 dB to accommodate an even greater range.

The worst case predetection signal-to-noise ratio due to the noise floor of the receiver can be determined from the block diagram. The minimum signal level in the Verification Receiver, -33 dBm, occurs at the input to the first amplifier following the mixer. This amplifier has a noise figure of 8 dB which results in a signal-to-noise ratio of 60 dB in a 20 MHz bandwidth. This value of signal-to-noise ratio insures that the post detection signal to noise ratios for FM and PM as specified in paragraphs 4.5.9.1(d) and 4.5.9.2(d) respectively would be met if the predominant source of noise were the receiver alone.

Two other sources of noise must be considered, however. These are the input phase noise from the exciter output and the Verification Receiver first L.O. Phase jitter on the S-Band exciter output is about 1 degree rms. Since the first L.O. of the receiver is derived from the exciter, its phase jitter should be essentially equal to that on the exciter output. If the noise from these sources were completely uncorrelated, then the total resultant phase jitter would be about 1.4 degrees rms and the SNR at the output of the PM demodulator given 1 radian peak modulation (40.5 degrees rms) would be 29.4 dB.

However, the power spectral density of the phase jitter is such that most of the noise, roughly 90 percent, lies within a frequency of ± 10 kHz about the carrier. Thus, provided the difference in time delay between the L.O. and input signal paths are not greatly different, less than 50 microseconds, the phase jitter on the two signals will be correlated to a large extent, and therefore, cancel.

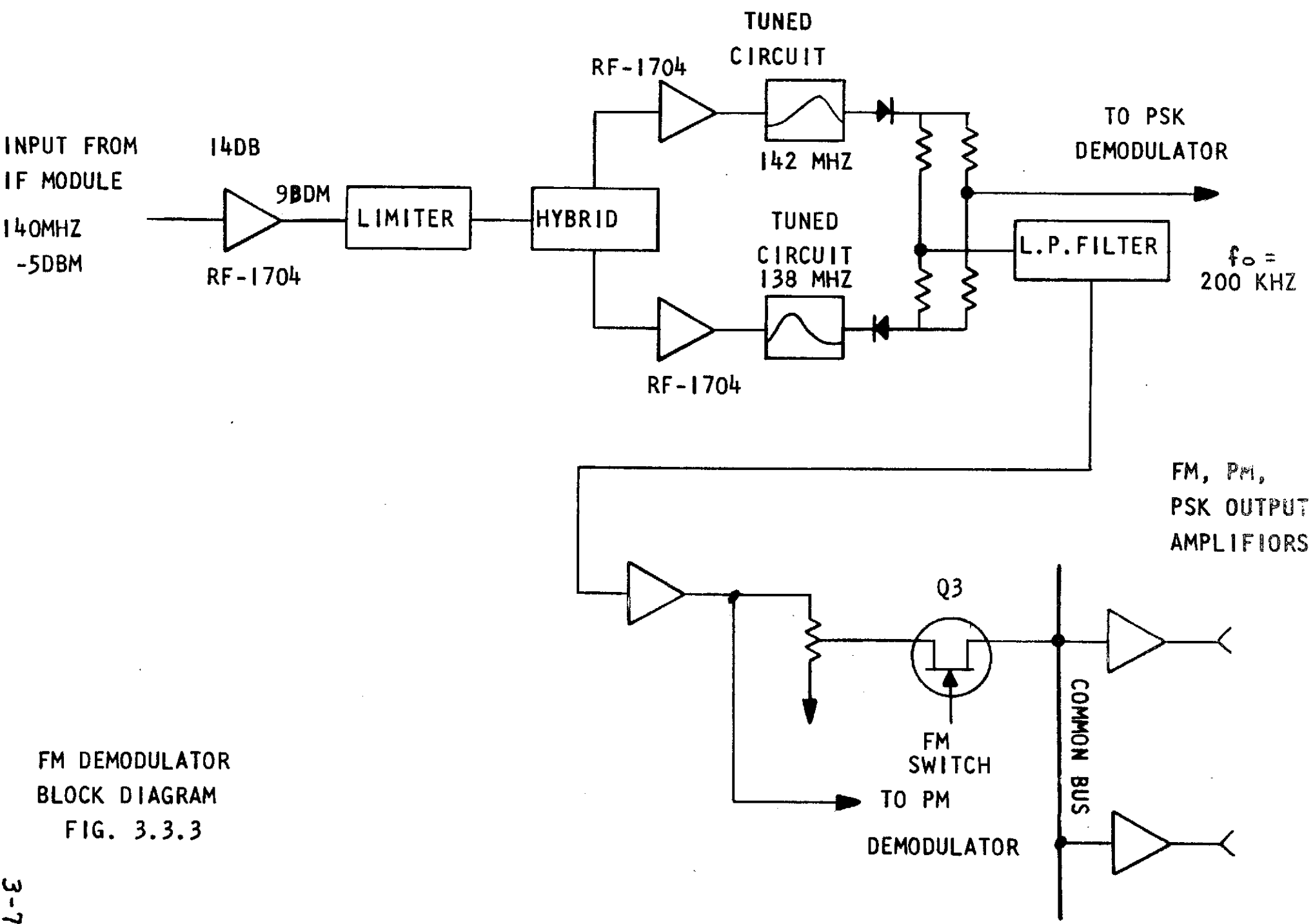
It is estimated that the degree of cancellation will amount to not less than 10 dB improvement over the case where noise is uncorrelated.

3.3.3 FM Demodulator

Figure 3.3.3 is a block diagram of the FM, PM, PSK demodulator module. The demodulated FM is used to derive both PM and PSK video as well as FM. The three types of demodulated output are switched so that the desired type is amplified by the two output amplifiers for two buffered outputs.

The 140 MHz input from the IF amplifier is amplified, limited, and applied to an LC frequency domain, or staggered circuits, discriminator. Peak-to-peak separation of the discriminator is 4 MHz which allows it to handle the 375 kHz peak deviation of the specified PM signal (3 radians peak at 125 kHz) with little distortion. The hybrid feeding the two tuned circuits avoids interaction when tuning the two circuits.

The discriminator output is filtered by a low-pass filter with a cut-off frequency of 200 kHz for both FM and PM. The signal is amplified for isolation purposes and a portion goes to FM gain control, R2. In the FM mode, Q3 switches the signal to the common bus and two output amplifiers to deliver 6 volts peak-to-peak to two 90 ohm loads.



FM DEMODULATOR
BLOCK DIAGRAM
FIG. 3.3.3

3.3.4 PM Demodulator

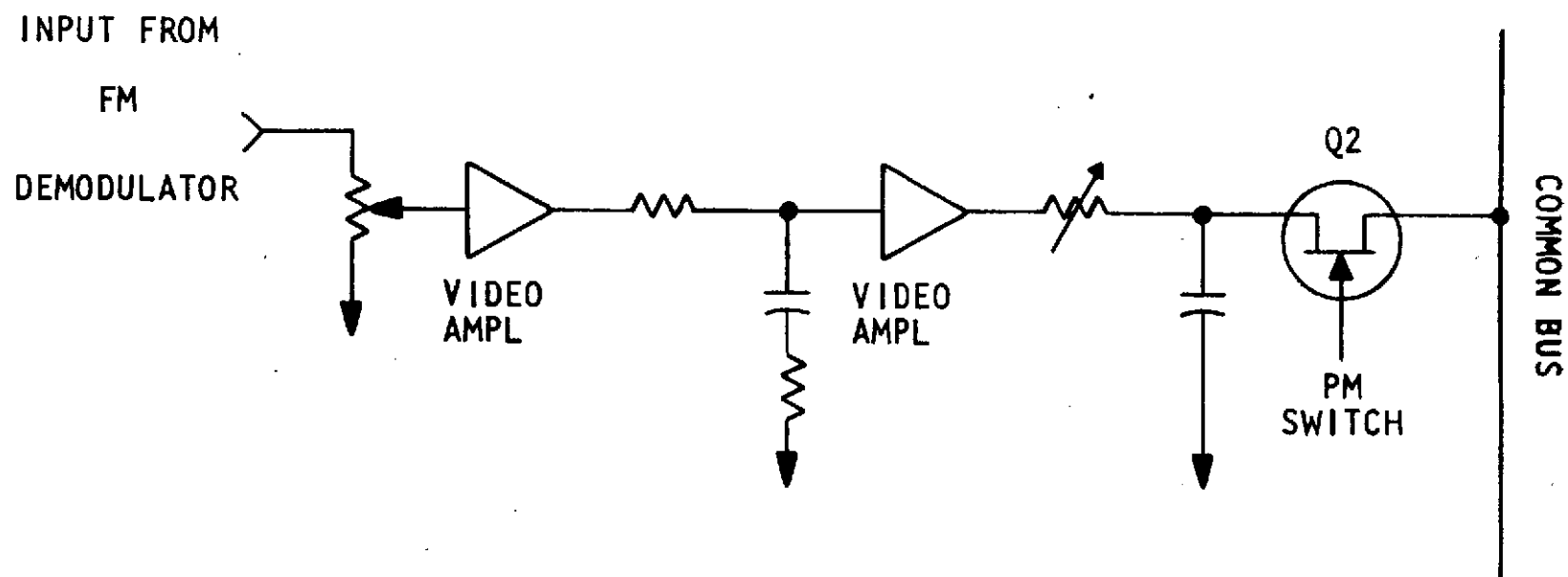
In order to keep the design of the Verification Receiver relatively simple and because the peak phase modulation specified is 3 radians, it was decided to use a non-coherent phase demodulator rather than a phase-locked loop system. Figure 3.3.4 is a block diagram of the proposed Phase Demodulator.

Phase modulation may be recovered from a PM signal by integrating the output of an FM discriminator. The Phase Demodulator performs this function in two stages. In principle, the process can be performed in a single stage, but considerations of circuit noise levels dictate otherwise.

The range of frequencies over which the integration must be performed is 100 Hz to 125 kHz, a ratio of 1250:1. High frequency signals would be attenuated severely with consequent degradation of signal-to-noise ratio. The use of two stages of integration as proposed reduces the amount of attenuation before re-amplification and avoids excessive degradation of SNR due to video noise.

The first integrator is a lead-lag network with a low-frequency break-point of 35 Hz and high-frequency break-point of 2.1 kHz. The break-point of the second integrator is 2.1 kHz and is adjustable so that an overall flat response may be obtained.

In the PM mode, Q2 switches the signal to the common bus and amplifiers used for the FM output.



PM DEMODULATOR
BLOCK DIAGRAM
FIG. 3.3.4

3.3.5 Phase Shift Keyed Demodulator

The PSK Demodulator makes use of the fact that the PSK Modulator is the same linear phase modulator used for PM (see 3.2.8). This means that in changing from -90° to $+90^\circ$ the signal temporarily increases in frequency to attain the new phase. The frequency deviation required depends upon the rise time of the PSK signal. Conversely, when the RF changes from $+90^\circ$ to -90° the frequency will temporarily decrease. The result is a plus spike in the FM demodulator for advancing phase and a minus spike for retarding phase.

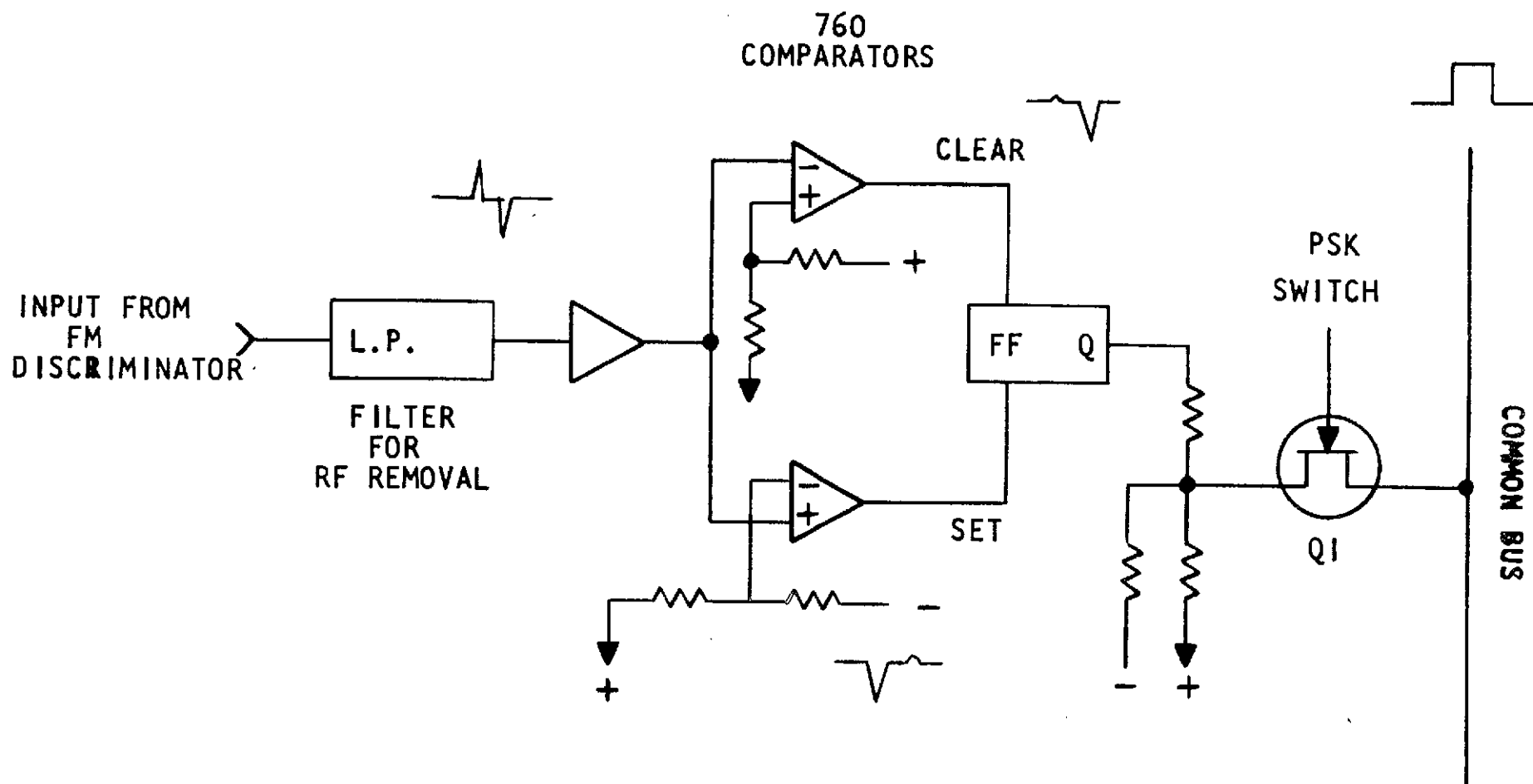
The FM discriminator output goes through a low-pass filter with a cut-off frequency above 10 MHz. This filter must be terminated so that it does not ring, or false pulses are generated. Two 760 comparators, AR6 and AR7, select the positive and negative spikes respectively. A logic zero for clear and reset respectively are generated.

The comparison levels are set to be sensitive to about 1/10 of the rise time expected for 500 kilobits split-phase. Thus lower rise times can be accommodated.

The spikes are used to clear and reset U1, an SN7474 FF. The Q output is set to logic zero for $+90^\circ$ and to logic 1 for -90° . This signal is divided by 20 and offset by a resistor network so that the common inverting X20 output amplifier will result in logic levels at the output. Here $+90^\circ$ will read logic 1 and -90° will read logic zero.

However, in order for the divided and offset signal to reach the common bus and common output amplifier, switch Q1 must be in the PSK mode (Q1 on).

This system is extremely simple, containing few elements. Hence the reliability will be excellent. This reliability is enhanced by the fact that a missed bit or gap in the signal will not invert the phase as might happen in the conventional squaring loop first proposed. The phase will also be correct the next time the equipment is turned on or a transmission starts.



PSK DEMODULATOR
BLOCK DIAGRAM
FIG. 3.3.5

3.4 Exciter Controls and Monitors

The exciter controls and indicators are located on four assemblies. These are:

1. Local Exciter Control - Contains exciter set-up and acquisition controls and monitors.
2. Local Test Control - Contains controls and monitors for testing the exciter system.
3. Remote Control - Contains acquisition controls and set-up monitors. This panel is designed to work with the Local Exciter Control or a computer to operate the exciter system.
4. Exciter Antenna Control - Contains controls to test the exciter system at the antenna.

The exciter system is designed to operate in one of three modes, selectable from the local control panel. These are:

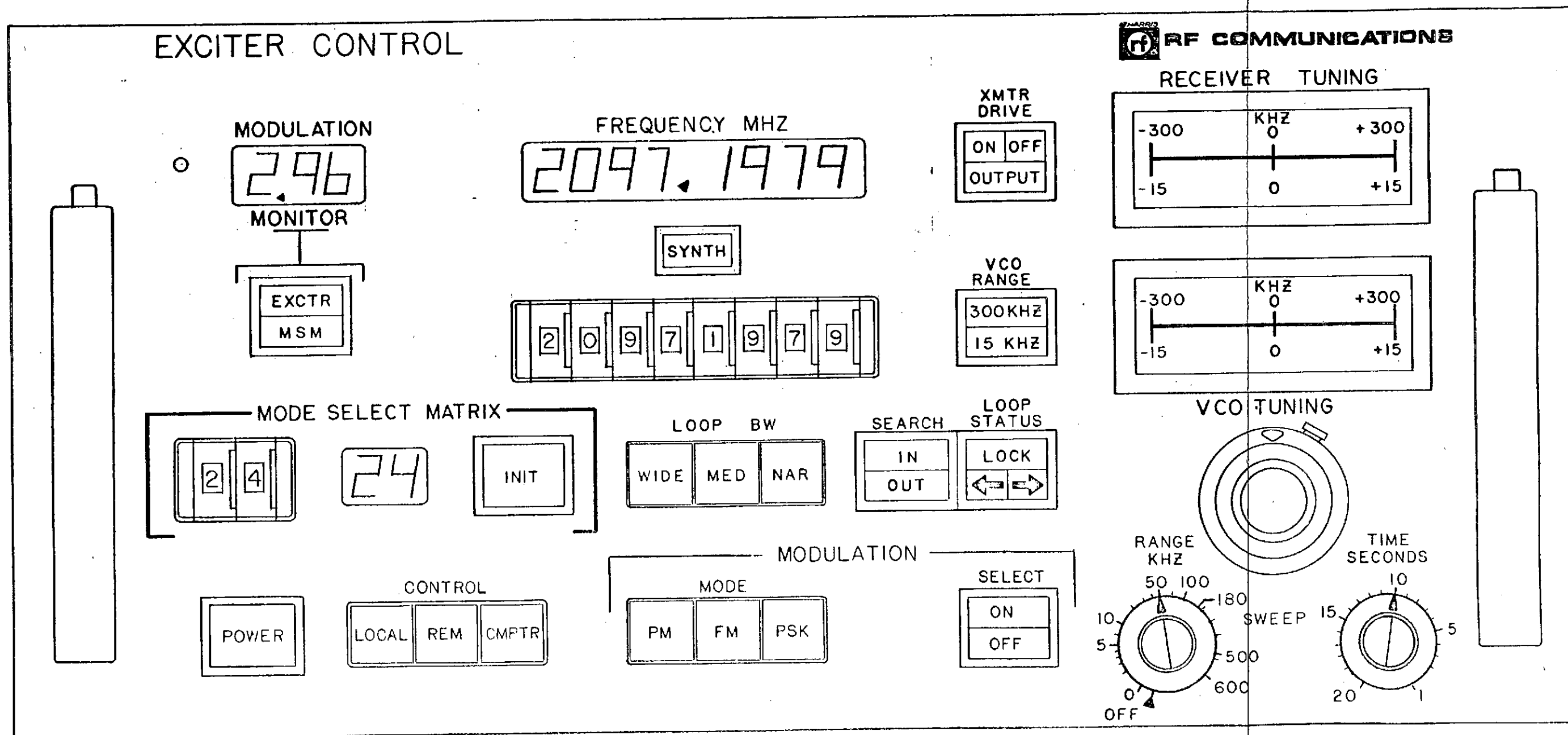
1. Local - all controls, set-up and acquisition, are selected from the local panel.
2. Remote - all set-up controls are selected from the local panel and all acquisition controls are selected from the remote panel.
3. Computer - All set-up controls are selected by a computer and all acquisition controls are selected from the remote panel.

In this system, "set-up" controls are FREQUENCY, MODULATION MODE, and LOOP BW. All other controls are "acquisition" controls. Test controls are local only.

3.4.1 Local Exciter Control

A layout of the Exciter Control panel is shown in Figure 3.4.1. The local Exciter Control is used to operate the exciter system when LOCAL control is used and provides "set-up" controls when REMOTE control is selected. The Exciter Control drawer provides the necessary interface for all REMOTE and COMPUTER controls (except for the VCO TUNING, SWEEP RANGE and SWEEP TIME which are selected in the exciter as described in section 3.2.5). All monitors remain active when REMOTE or COMPUTER control is selected. A brief description of the front panel controls follows.

1. Power - Switch/indicator provides primary power to the DC power supplies for the rack mounted equipment.
2. Control Mode - Switch/indicator selects the three control modes LOCAL, REMOTE, or COMPUTER.
3. Exciter Frequency - Thumbwheel switch selects exciter operating frequency in LOCAL or REMOTE modes.
4. Frequency Display - Indicates exciter operating frequency in all control modes.
5. Search - In/Out - Switch/indicator enables frequency search about the selected carrier frequency (IN). Removes search and enables the phase lock loop which locks the search VCXO to the frequency standard (OUT).
6. Loop BW - Switch/indicator - Three positions which select the search VCXO phase lock loop bandwidth (WIDE, MED, NAR).



S-BAND EXCITER
 EXCITER CONTROL PANEL
 FIG. 3.4.1

7. Loop Status - Indicator shows phase lock of the search VCXO in the search mode.
8. VCO Range - Switch/indicator selects the search range of the VCXO, ± 300 kHz or ± 15 kHz.
9. Exciter Tuning - Meter indicates the relative frequency of the exciter search VCXO.
10. Receiver Tuning - Meter indicates the relative frequency of the ground receiver VCXO.
11. Synthesizer - Indicates a fault in the frequency synthesizer.
12. VCO Tuning - Ten turn potentiometer with counter dial. Provides for manually offsetting the search VCXO.
13. Sweep Range (kHz) - Calibrated Dial/Potentiometer adjusts the sweep search range from 0 to 600 kHz.
14. Sweep Time (sec) - Calibrated Dial/Potentiometer adjusts the rate of search by varying the time to sweep search the selected range.
15. XMTR Drive - Switch/indicator provides control to the Antenna Control Panel for energizing the transmitter, Indicates OUTPUT when exciter drive is adequate.
16. Modulation Monitor - Digital panel meter indicates 0.00 to 3.00 volts corresponding to 0 to 3 radians PM index or 0.00 to 1.00 volts corresponding to 0 to 1.0 MHz FM deviation.
17. Mode Select Matrix - Group of controls and indicators to monitor and control the Mode Select Matrix.

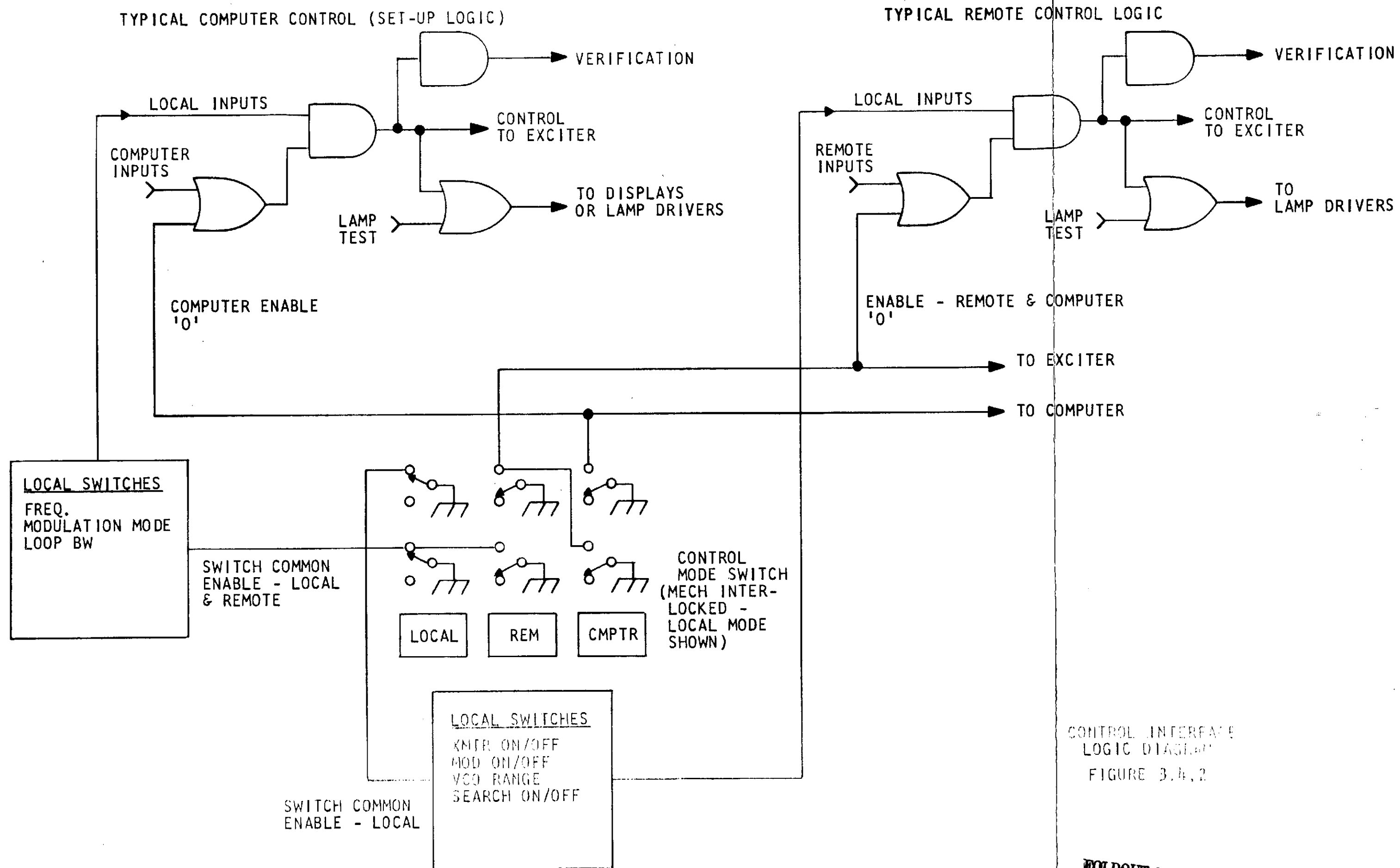
The controls include:

- a. Thumbwheel switch which provides decimal (0 to 99) information to the MSM.
 - b. Indicator to monitor the MSM status.
 - c. EXCITER/MSM - Switch indicator to control the input to the Modulation Monitor. The exciter position indicates a composite modulation index and the MSM indicates the individual modulation indices.
 - d. INITIATE - Momentary switch/indicator to command on the MSM.
18. Modulation - Two Switch Indicators to control and monitor the Exciter modulators. The controls are:
- a. SELECT ON/OFF - Switch indicator to enable or disable the modulators in the LOCAL control mode.
 - b. MODE - Switch Indicator to select the modulator (PM, PSK or FM) in the LOCAL or REMOTE control mode.

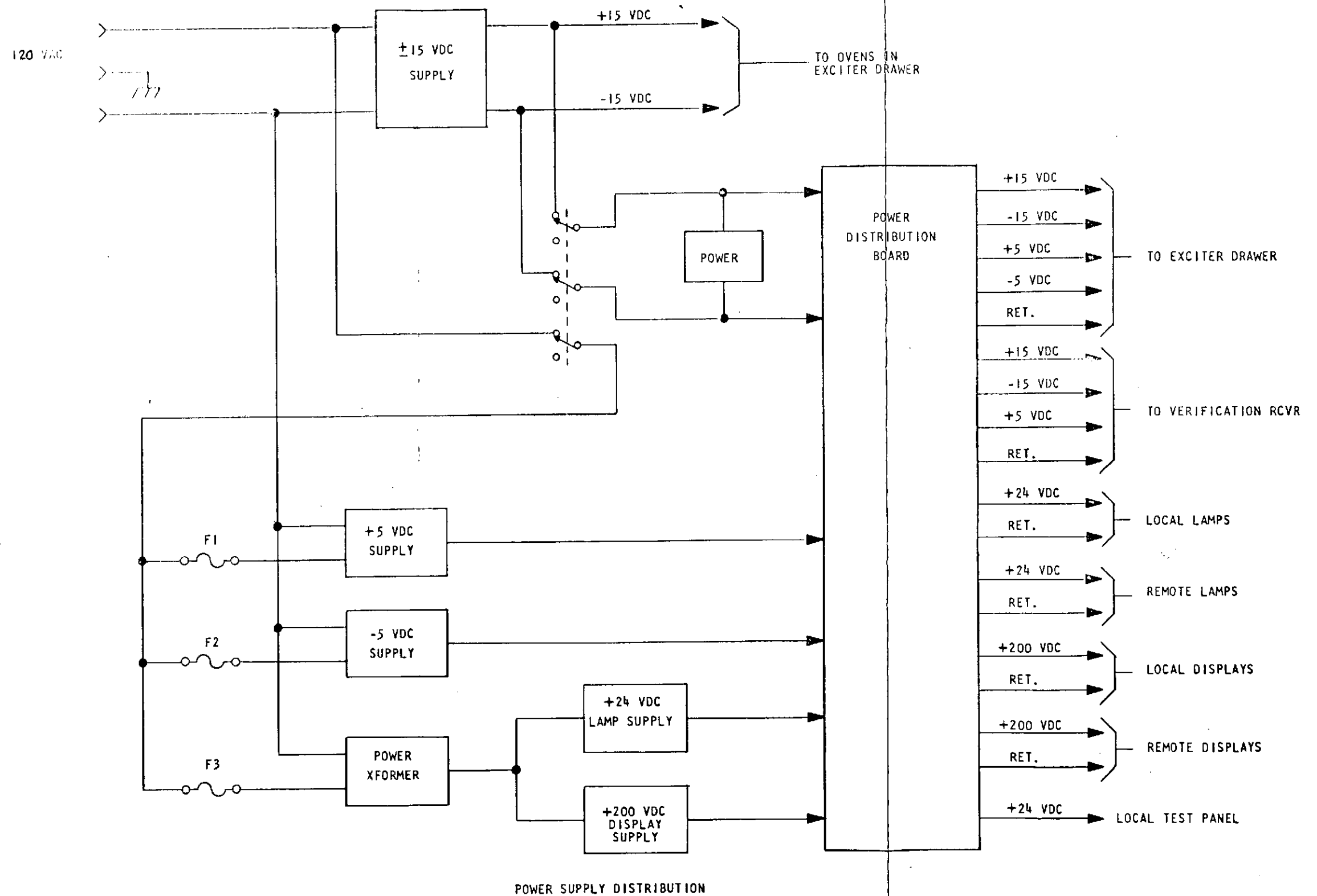
Figure 3.4.2 illustrates how the COMPUTER control feature is implemented. Three functions, FREQUENCY, MODULATION MODE and LOOP BW are computer selectable in the COMPUTER mode. All other controls come from the Remote Control panel.

Figure 3.4.2 also illustrates how the REMOTE control feature is implemented. The Remote Control lines are active when REMOTE or COMPUTER control mode is selected. In REMOTE the FREQUENCY, LOOP BW and MODULATION MODE are controlled locally.

Figure 3.4.3 is an overall block diagram of the Exciter Control drawer. In addition to the control logic boards, the



CONTROL INTERFACE
 LOGIC DIAGRAM
 FIGURE 3.4.2



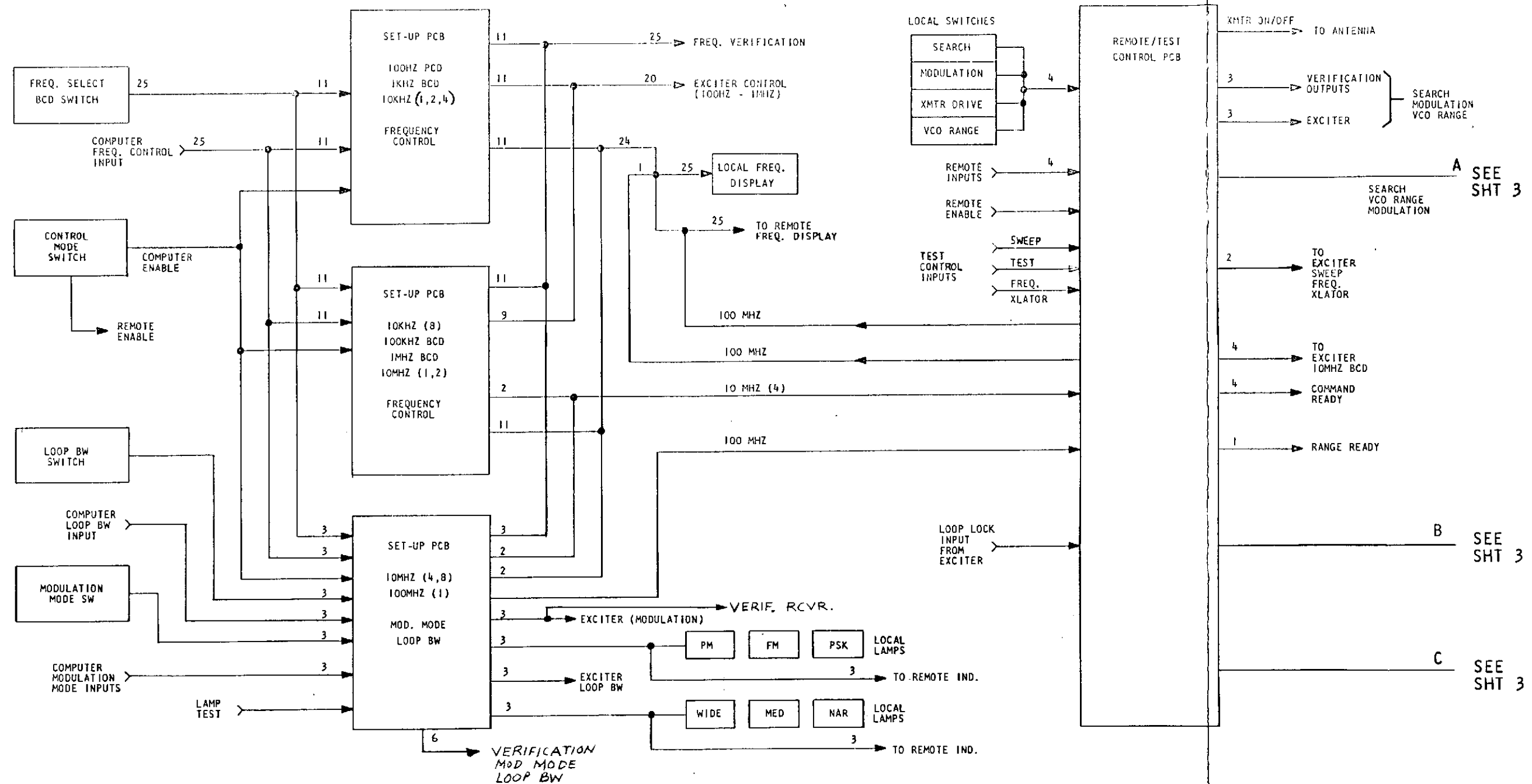
EXCITER CONTROL DRAWER
BLOCK DIAGRAM

FIGURE 3.4.3
SHEET 1 OF 3

FOLDOUT FRAME 1

FOLDOUT FRAME 2

3-89-A



EXCITER CONTROL DRAWER
BLOCK DIAGRAM
FIGURE 3.4.3
SHEET 2 OF 3

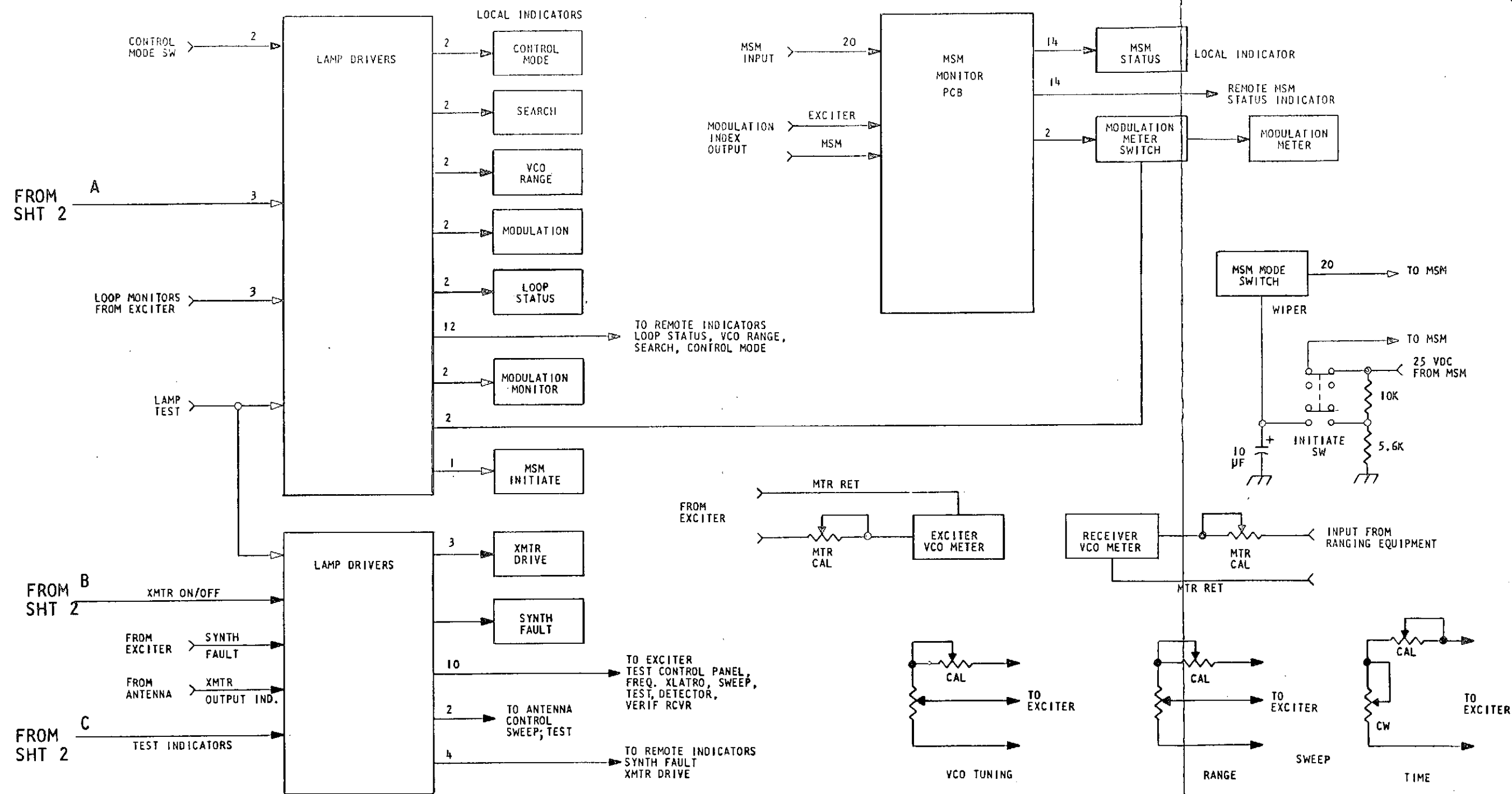
3-89-B

FOLDOUT FRAME /

FOLDOUT FRAME 1

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EXCITER CONTROL DRAWER
BLOCK DIAGRAM
FIGURE 3.4.3
SHEET 3

3-89-C

FOLDOUT FRAME

FOLDOUT FRAME

DC power supplies for the Operations Building equipment are located in the control drawer.

Control lines are processed in the set-up and Remote/Test control boards and distributed to the exciter, the indicator lamp driver boards and the display boards. The 10 MHz frequency information is processed in the Remote Control/Test board to provide the synthesizer with proper tuning information. The synthesizer is designed to operate over a 25 MHz range (100 MHz after multiplication) if operated directly from the BCD switch. A binary adder and binary to BCD converter provide the proper code to the synthesizer to tune 23.75 MHz (95 MHz after multiplication).

The status lines from the MSM, which are decimal, are converted to seven-line codes to drive the MSM status indicators.

3.4.2 Test Controls

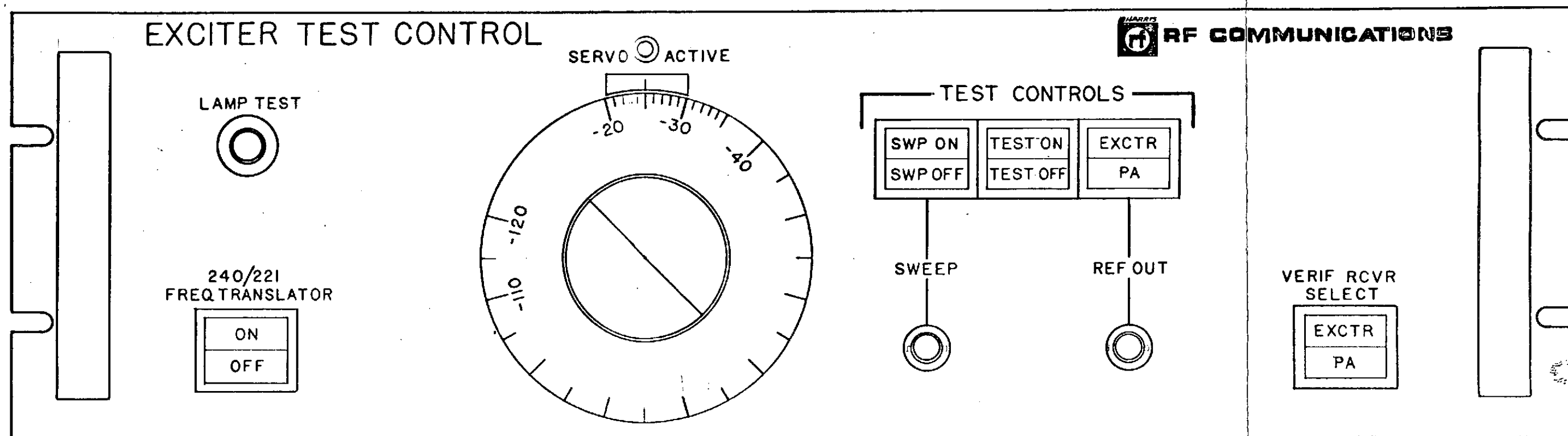
Provision is made for testing the exciter from one of two test control panels. One is located in the Exciter rack below the Exciter Control and the other is located at the antenna in the S-Band Amplifier rack.

Test features include sweeping the exciter frequency for bandpass testing the Exciter 16 Watt Amplifier/multiplier or the S-Band Power Amplifier. Sweep return blanking is employed on the detected output. Also, a 240/221 Frequency Translator can be selected from the local Test Panel to test the exciter/ground receiver system. A servo driven attenuator varies the translator output from -20 to -120 dBm.

3.4.2.1 Local Exciter Test Control Panel

Figure 3.4.4 is a layout of the Exciter Control Panel in the Exciter Rack. A brief description of the controls follows.

1. Lamp Test - Momentary switch - Allows testing of all lamps on the Exciter Control, Remote Control and the Local Test Control.
2. 240/221 Frequency Translator - Switch/Indicator - Enables the Frequency Translator when TEST ON is selected. A remote control dial which acts as the transmitter unit for a servo positioner which in turn controls the Frequency Translator output attenuator.
3. SWP ON/OFF - Switch/Indicator - Enables the sweep generator which continuously tunes the exciter for band-pass testing the system in TEST ON. This switch is wired in a "three-way-switch" configuration with the SWP ON/OFF switch in the Antenna Test Control.
4. Test On/Off - Switch/Indicator - Enables the test functions of SWP ON/OFF and FREQ. TRANSLATOR ON/OFF. This switch overrides the other test controls.
5. Exciter/PA - Switch/Indicator - Select either the detected output of the Exciter Amplifier or the Power Amplifier to the front panel BNC connector.
6. Verification Receiver Select - Switch indicator - selects input to the verification receiver - either the 16 watt amplifier or the power amplifier.



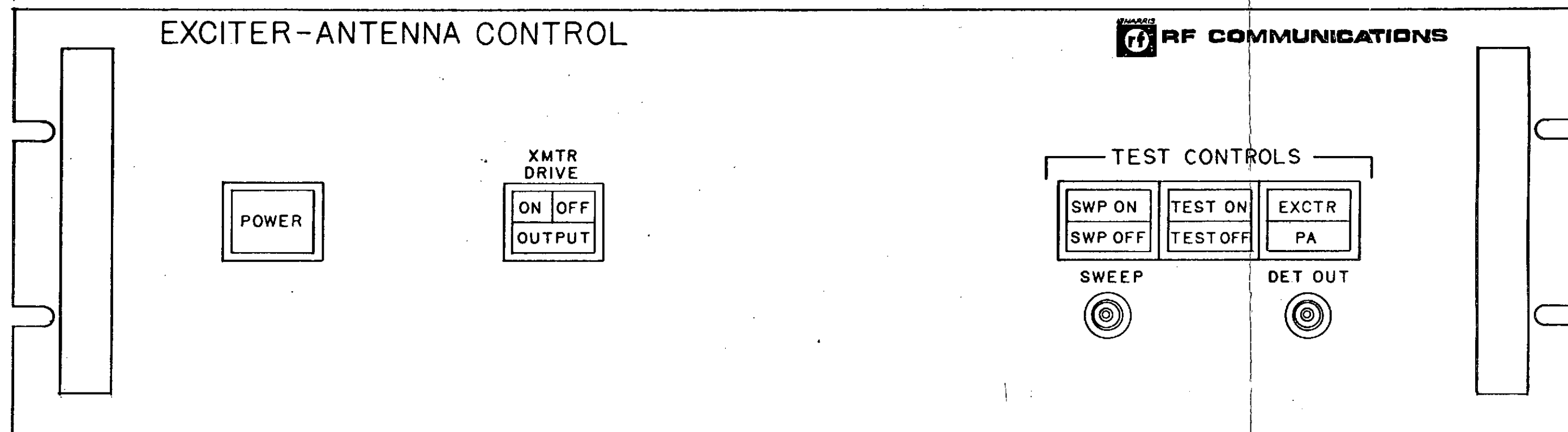
S-BAND EXCITER
TEST CONTROL PANEL
FIG. 3.4.4

3.4.2.2 Antenna Control

Figure 3.4.5 is a layout of the Antenna Control Panel. The following controls are included.

1. Power - Switch/Indicator - Provides power to the Antenna electronics subsystem.
2. Xmtr Drive - Switch/Indicator - Same function as the switch on the Local and Remote Exciter Control panels. However, this switch overrides the others and provides a positive off.
3. SWP On/Off - Switch/Indicator - Identical to the switch on the Local Test Control Panel.
4. Test On/Off - Indicator - Indicates the status of the TEST ON/OFF switch on the Local Test Control Panel.

The local and antenna control panels are used together and the extent of their interdependence can be understood by studying figure 3.4.6. As indicated previously, the local TEST ON mode must be selected to use the SWEEP function locally or from the antenna. The SWEEP function can be controlled from either position. The TEST mode is disabled when REMOTE or COMPUTER Control mode is selected.



S-BAND EXCITER
ANTENNA CONTROL PANEL
FIG. 3.4.5

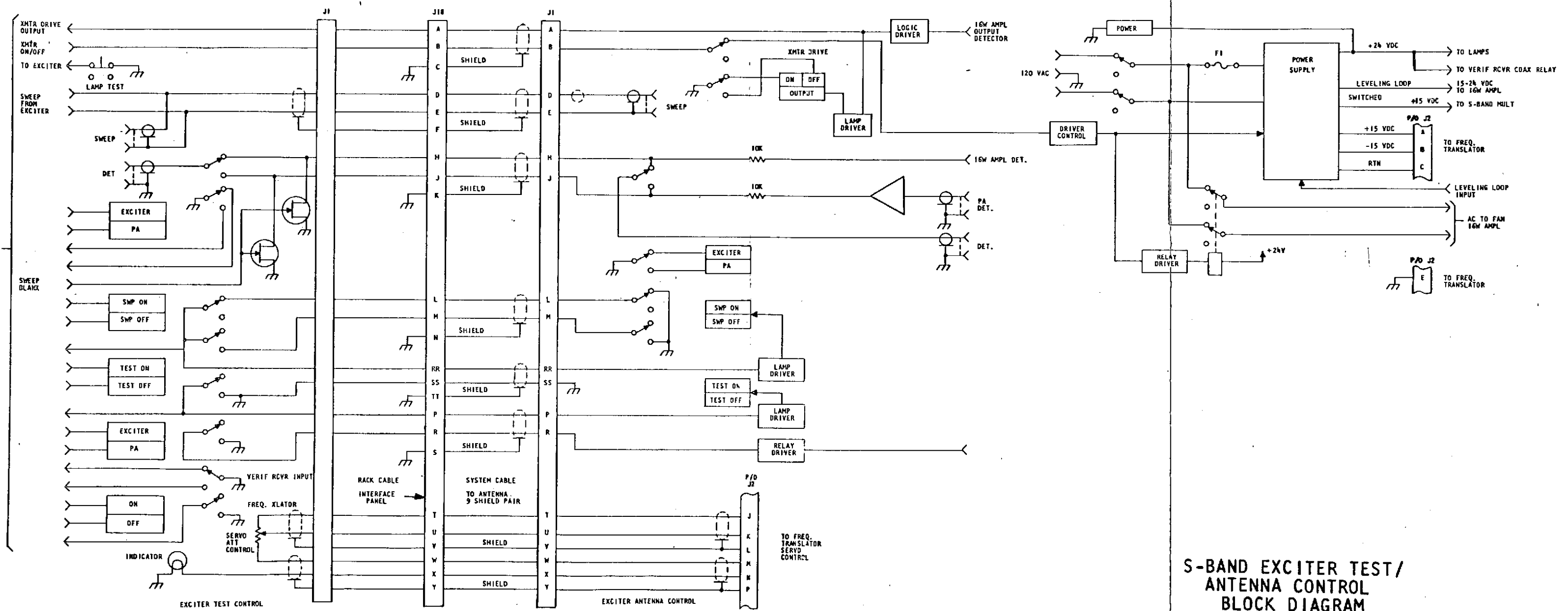
3-95

FOLDOUT FRAME /

FOLDOUT FRAME 12

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S-BAND EXCITER TEST/
ANTENNA CONTROL
BLOCK DIAGRAM
FIGURE 3.4.6

3-96

FOLDOUT FRAME 1

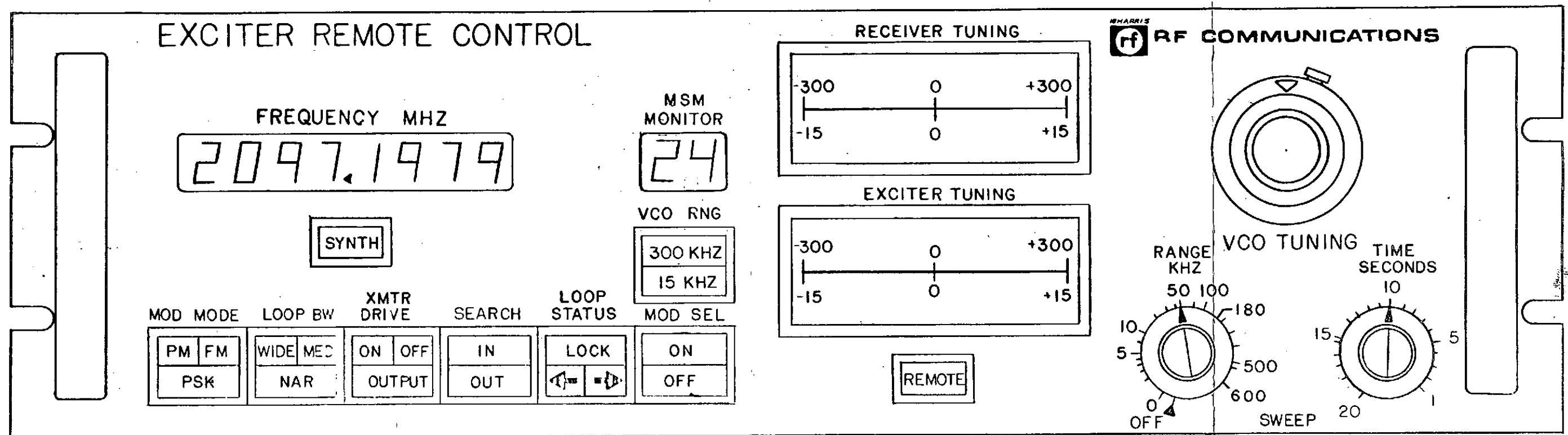
FOLDOUT FRAME 2

3.5 Remote Control Panel

Figure 3.5.1 is a layout of the Remote Control panel. The panel arrangement is similar to that used in the local control.

The controls and indicators are the same except that:

1. No FREQUENCY selection is provided; however the exciter frequency is presented on the same type of display.
2. NO MODULATION MODE selection is provided; however, a lighted indicator displays the selected modulation mode.
3. Mode Select Matrix Controls are omitted.
4. The digital panel meter is omitted.
5. Test Controls are omitted.
6. An indicator displays Control mode status when REMOTE is selected at the local panel.



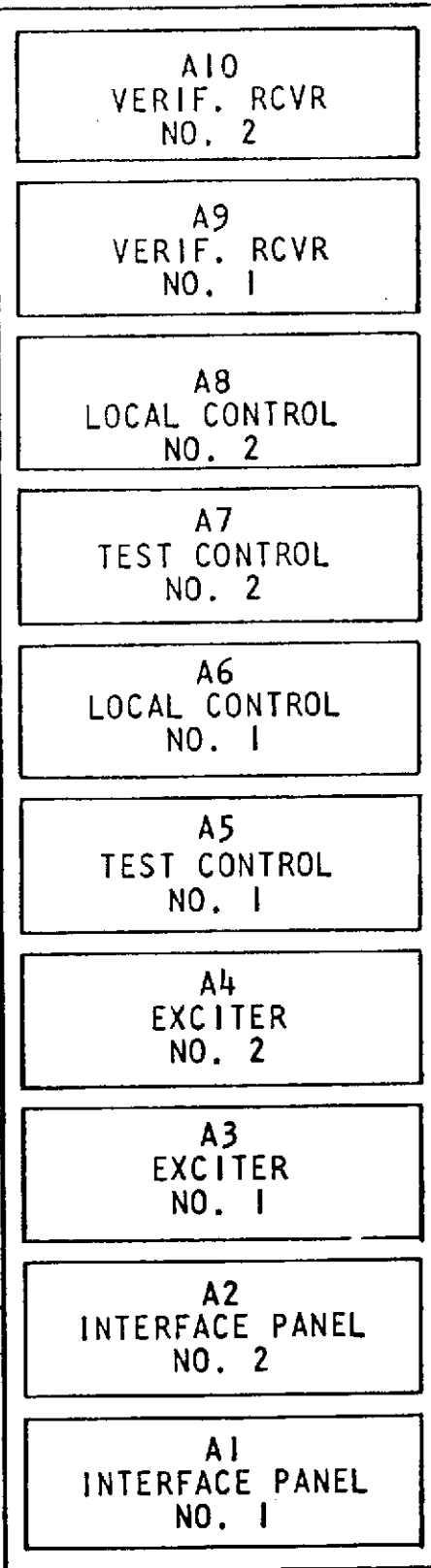
S-BAND EXCITER
REMOTE CONTROL PANEL
FIG. 3.5.1

3-98

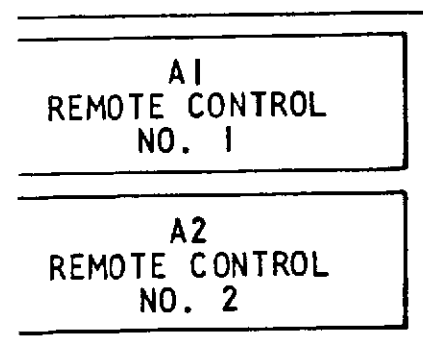
3.6 System Interface

Figure 3.6.1 shows a typical installation including two exciter systems. System reference designations are shown on each major assembly. Figures 3.6.2 and 3.6.3 show the control and RF interconnecting cables. In addition to the remote control and antenna control cables outputs, isolated verification outputs are provided at each of two connectors. Standard TTL voltage outputs are provided. Also, a "COMMAND READY" output is supplied. This signal is an "AND" function of XMTR ON, MODULATION ON, and SEARCH OUT. A "RANGE READY" signal is also provided which is an "AND" function of "COMMAND READY" and LOOP LOCK (search VCXO phase lock).

UNIT NO. 1

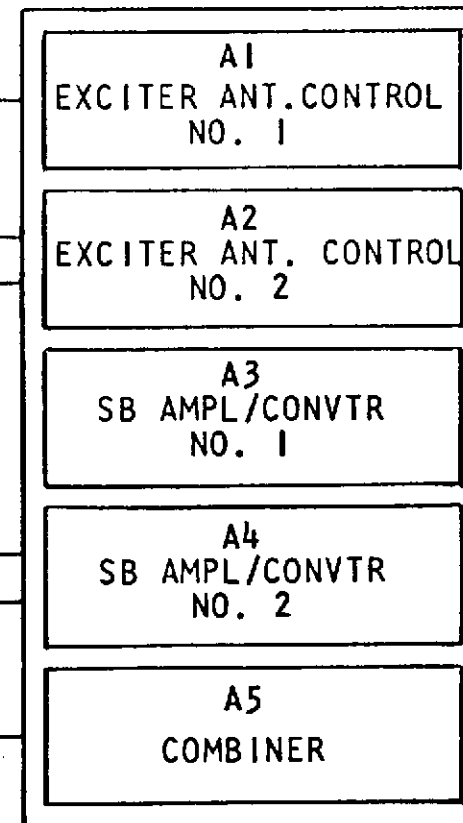


UNIT NO. 2



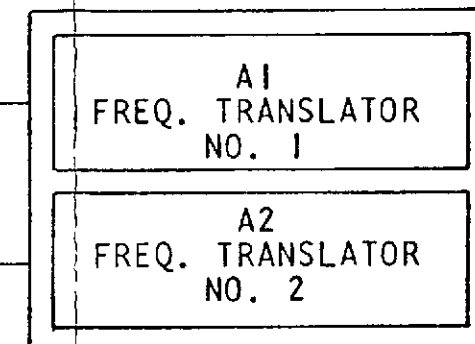
COMPUTER CONTROL

UNIT NO. 3



2025-2120 MHZ OUT

UNIT NO. 4



2200-2300 MHZ OUT

2025 - 2120 MHZ OUT

FOLDOUT FRAME 2

S-BAND EXCITER SYSTEM
(2 EXCITERS)
BLOCK DIAGRAM

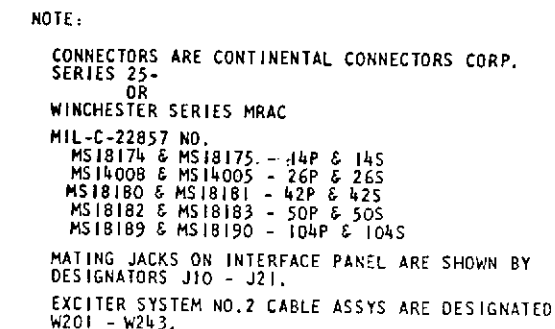
FIGURE 3.6.1

3-98 B

FOLDOUT FRAME 1

FOLDOUT FRAME

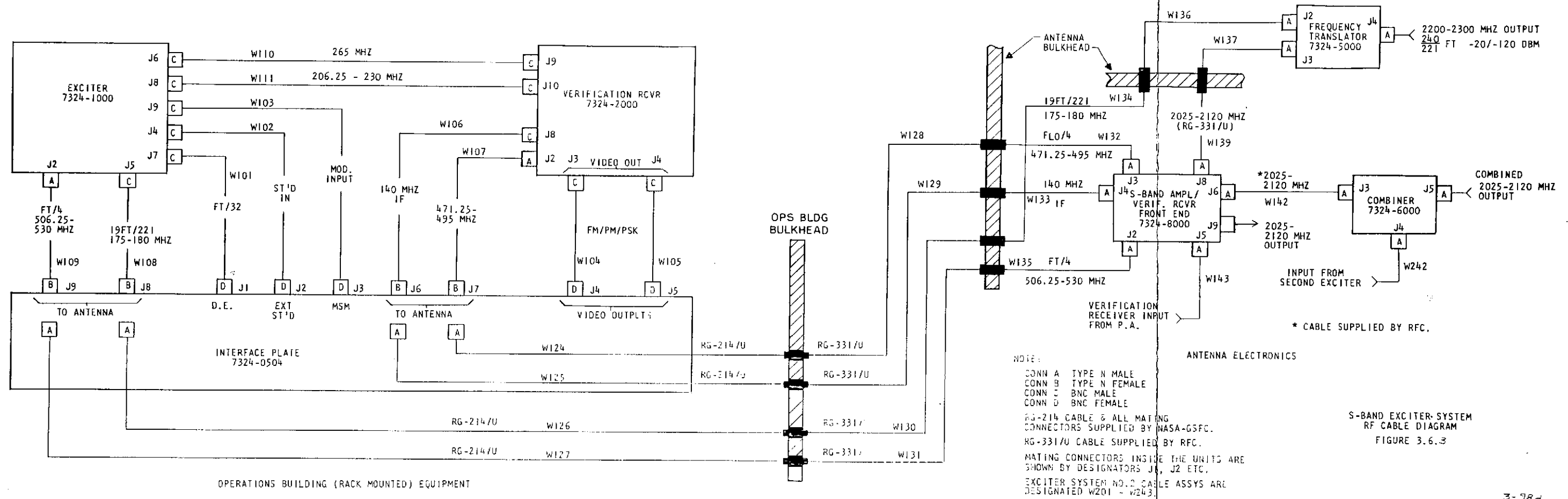
FOLDOUT FRAME 2



3-92 c

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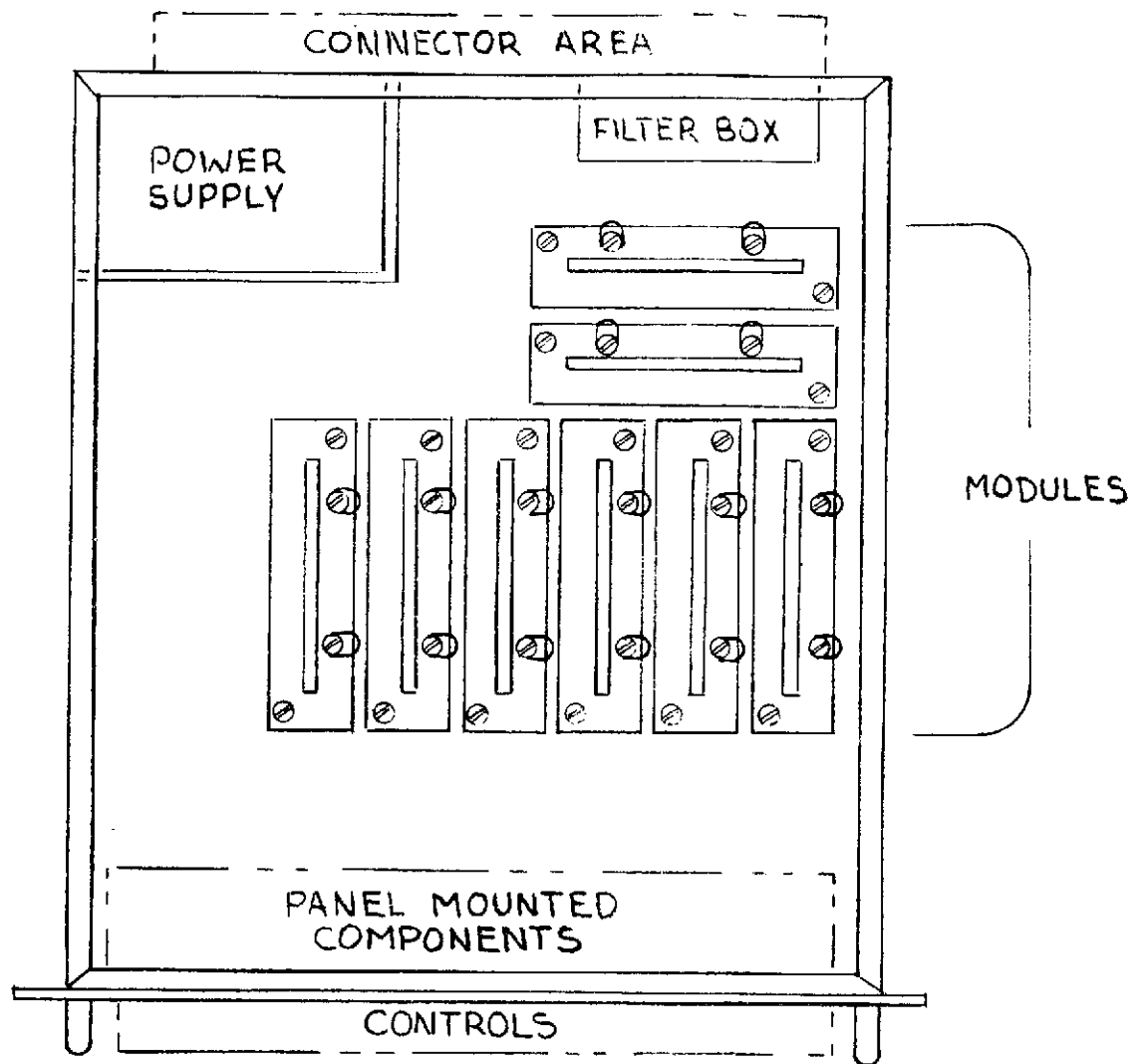
FOLDOUT FRAME 1

FOLDOUT FRAME 2

3.7 Exciter Subsystem Mechanical Design

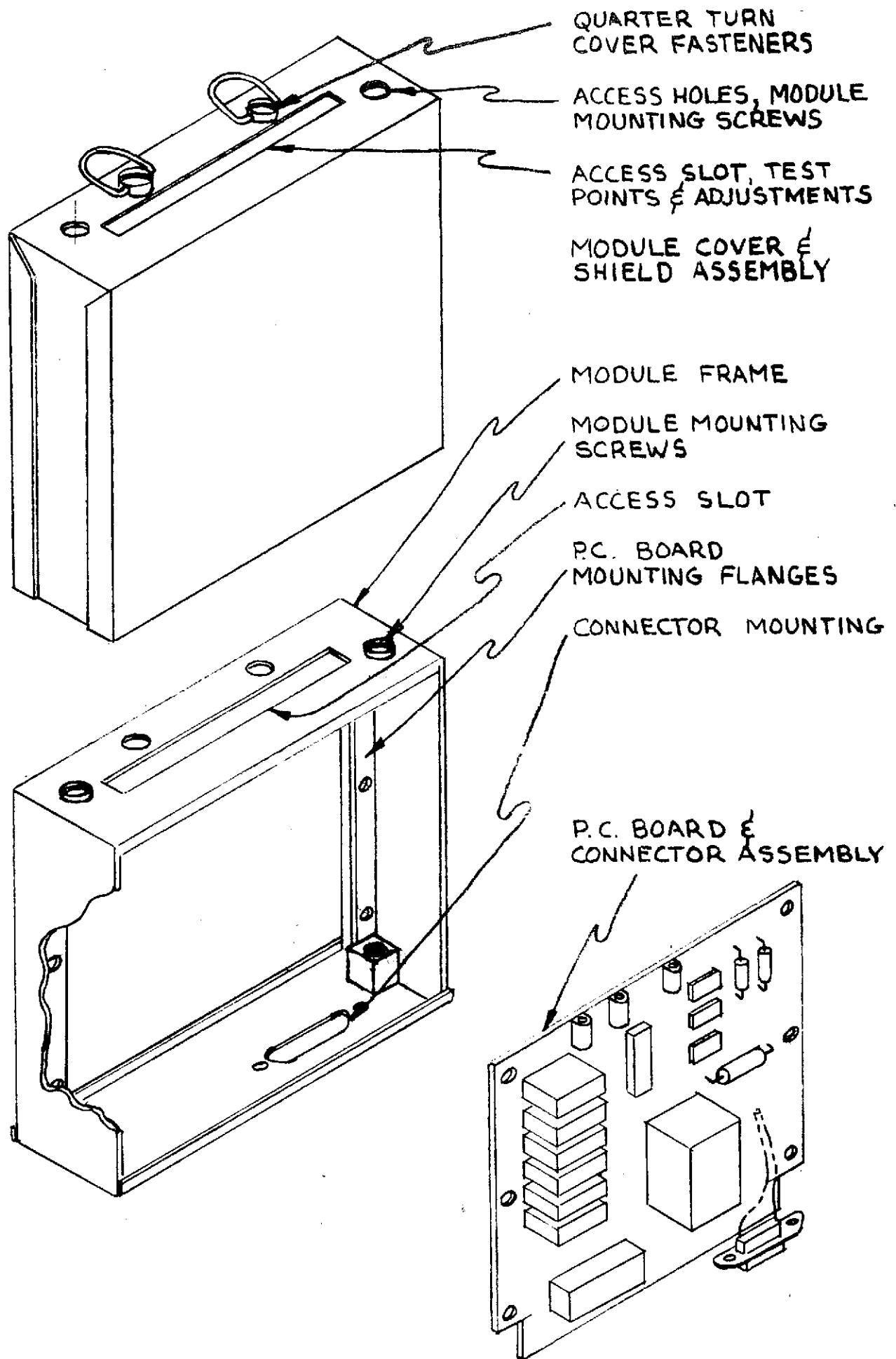
Typical design and layout of the drawer mounted equipment is shown in Figure 3.7.1. The drawer frame is a sheet metal fabrication using wrap around construction with cover mounting flanges formed inward on all four edges of the drawer, both top and bottom. All corner seams at the interface of the flanges are fillet welded and ground flush to provide an inherently RFI tight enclosure. Both top and bottom covers incorporate a sufficient number of fasteners used to assure an RF tight interface. A shelf in the lower portion of the drawer affords mounting provisions for the modules and their associated connectors. The area between the shelf and the bottom cover is used for the necessary drawer interconnecting cabling. Connections to other equipments are provided for by rear panel mounted connectors.

Module construction, depicted in Figure 3.7.2, features a dip brazed rectangular structure approximately 6 x 6 x 1-3/4 inches. A vertical flange along each side of the frame provides mounting points for the printed circuit card assembly. The connector, located on the bottom surface of the module, interfaces with its associated connector mounted on the drawer shelf. Two through bolts, readily accessible from the top of the module provides for rapid installation or removal. The cover is an open ended box structure that slides over the frame and is secured by two quarter turn fasteners located on the top surface of the cover. The fasteners incorporate a pull ring that serves as an aid in extracting the module. A slot along the top of the cover and frame yields ready access to test points and adjustments.

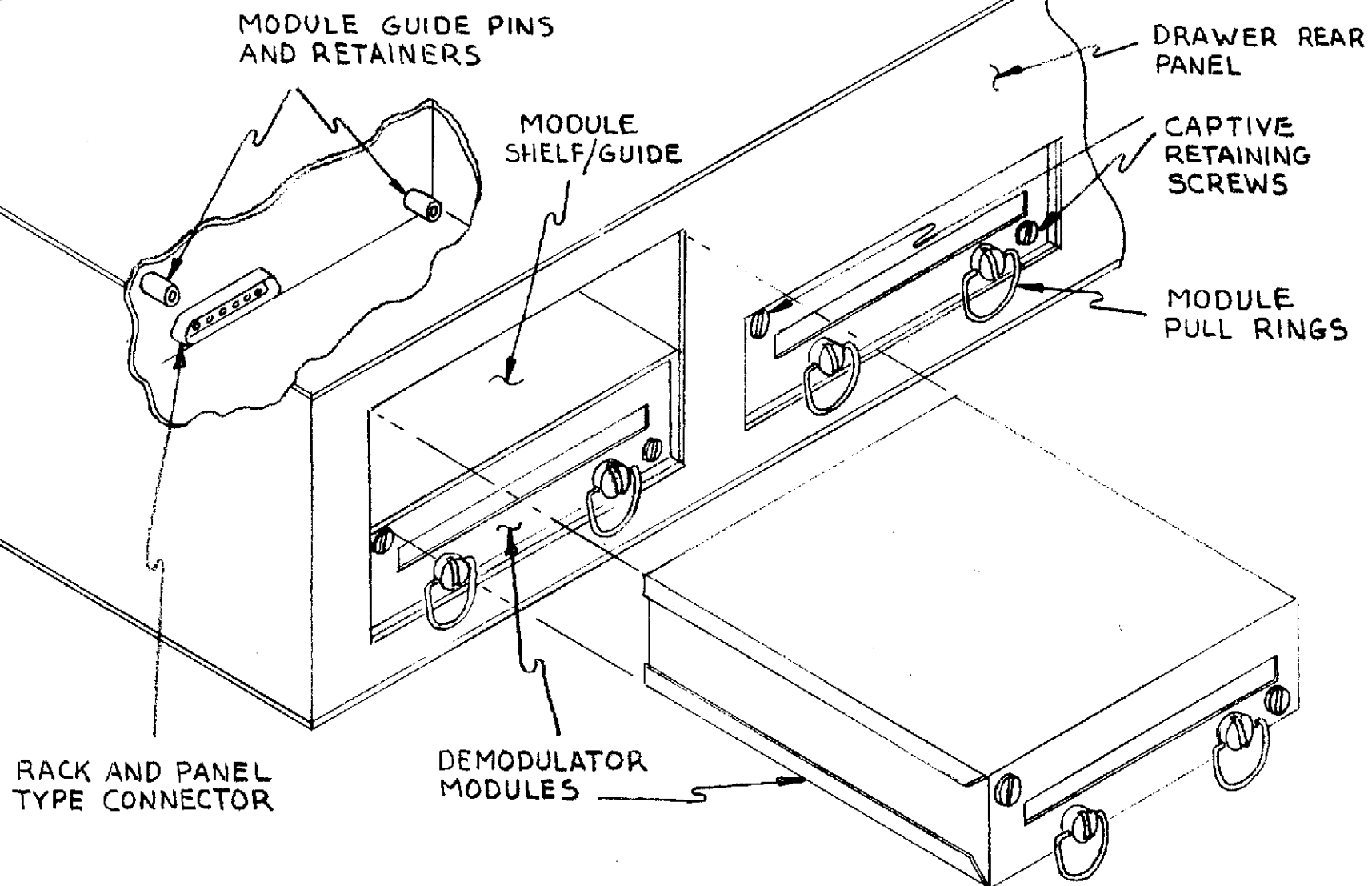


TYPICAL DRAWER
LAYOUT

FIGURE 3.7.1



The demodulator modules, constructed as described above, are easily installed or removed from the rear of the rack as shown in Figure 3.7.3. Cavities in the rear panel of the drawer contain a shelf which acts as the initial alignment guide for the module. Upon full insertion, guide pins located at the base of the cavity engage locating holes in the base of the module assuring proper mating of the connectors. The module is retained in the cavity by the two captive through bolts.

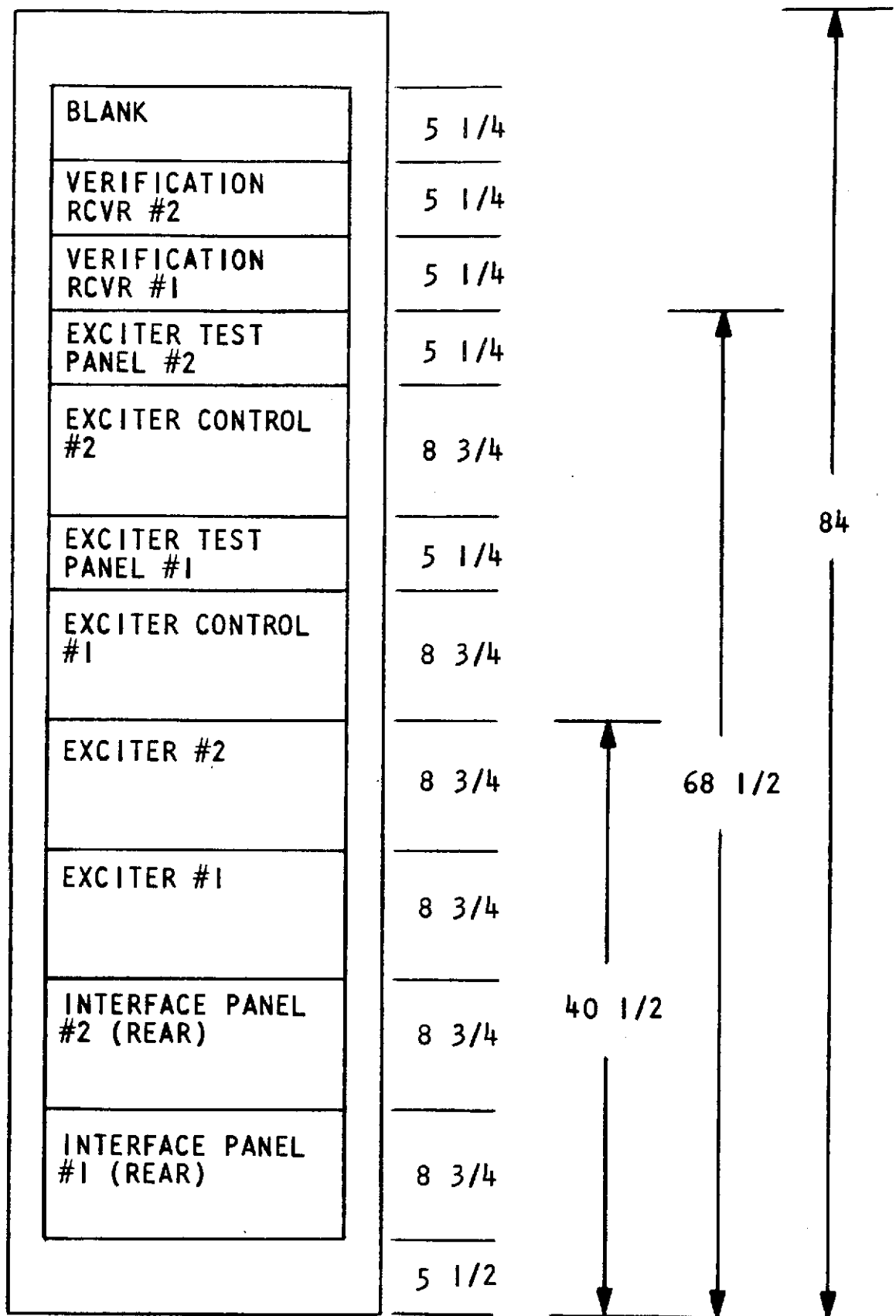


DEMODULATOR MODULE
INSTALLATION

FIGURE 3.7.3.

3.7.1 Exciter Rack Layout

The Exciter rack layout and panel dimensions are shown in Figure 3.7.4. This configuration has been chosen to place operating controls and indicators, for both exciters, on the front panel, at a convenient height for a standing operator - that is, between about 40 and 68 inches above the floor. The rack structure is in accordance with GSFC-S-572-P-2C for 19 inch panels, and is essentially identical to the MFR rack. The two identical interface plates are mounted in bottom rear of the rack, about 8 inches from the rear of the rack.



(APPROX. DIMENSIONS IN INCHES)

EXCITER RACK LAYOUT

FIGURE 3.7.4

3.8 Antenna Equipment

The antenna equipment refers to the following three assemblies.

1. Antenna Electronics: An assembly, rack mounted on slides, to be normally located in the "wheel house". This assembly contains two X4 multipliers, the verification receiver down converter, the 16 watts S-Band amplifier. The supply connections to these units are from the antenna control panel. For thermal considerations provisions are made to install a fan to cool S-Band amplifier assemblies.

2. Translator: A pressurized assembly made for mounting at the antenna feed point, but also adaptable to rack mounting.

3. Output Combiner: A rack mounted assembly containing two power attenuators, hybrid and bypass control switch. This unit to be mounted adjacent to a pair of antenna electronics units in the "wheel house".

3.8.1 Antenna Electronics

Figure 3.8.1 is a block diagram of antenna electronics assembly. The upper portion of the diagram pertains to verification receiver front end while the lower portion pertains to S-Band power amplifier. The transmit band signals (2025-2120 MHz) from either the exciter or from the Klystron output are selected by a relay and mixed to a fixed IF of 140 MHz.

The signals (506.25 - 530 MHz) from the exciter are filtered for spurious response and multiplied to S-Band (2025 - 2120 MHz) to +23 dBm nominal level. These signals are first amplified by a driver amplifier to +38 dBm level and then by a power amplifier to +43 dBm. The power amplifier is followed by an isolator for open or short circuit protection, a low pass filter to reduce the harmonic distortion and a directional coupler. The directional coupler has three sampled outputs. The first output which is 33 dB below S-Band power output is sent to the verification receiver down converter via a relay and a band pass filter. The second output is the detected sweep which is also used for the leveling control. The third output goes to the frequency translator through a selected pad.

The sampled PA input from the Klystron is sent to the verification receiver down converter through a selected pad, relay and a band pass filter. The selection of PA or exciter input is made by a coaxial relay which is controlled by lighted push-button switch on the local test control panel. The "PA" position is the normal or de-energized position for the coaxial relay.

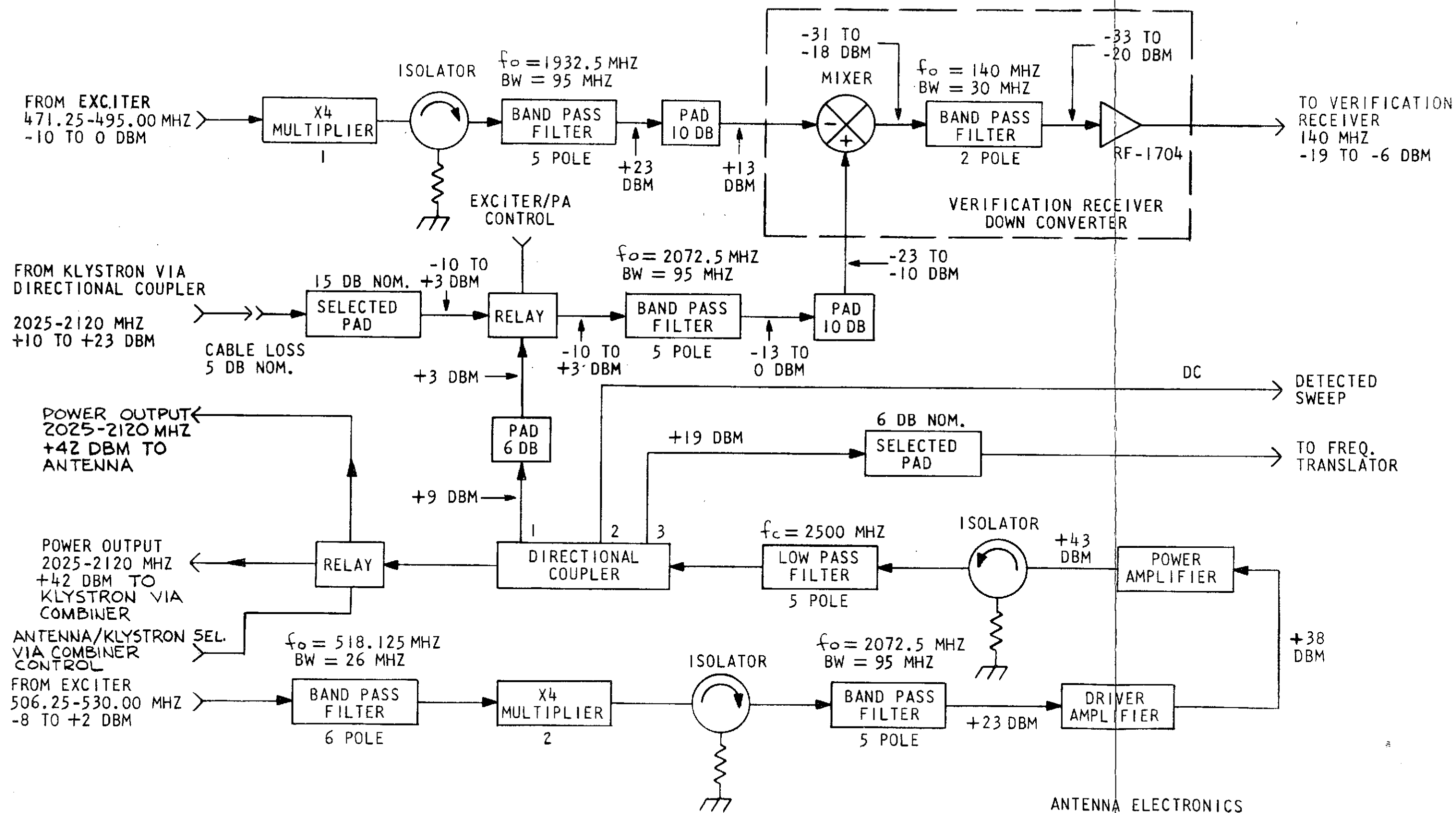
The output of the S-Band power amplifier is switched

between antenna and Klystron (via combiner) by a coaxial relay operated by +24 volts supply. The normal or de-energized position of the relay selects the Klystron.

The signals (471.25 - 495 MHz) from the L.O. translator are multiplied to S-Band (1885 - 1980 MHz) and sent to the verification receiver down converter as L.O. at +13 dBm level. The output of the quadrature hybrid mixer is sent to the verification receiver through a band pass filter and an amplifier.

The antenna test panel contained in this assembly will provide plus and minus 15 volts to run operational amplifiers, +15 V to power X4 multipliers, +24 V for relay operation and one or more adjustable voltages between +20 and +28 volts to operate the S-Band driver and power amplifier. The adjustable voltage on the power amplifier will be controlled to provide automatic power control of the RF output.

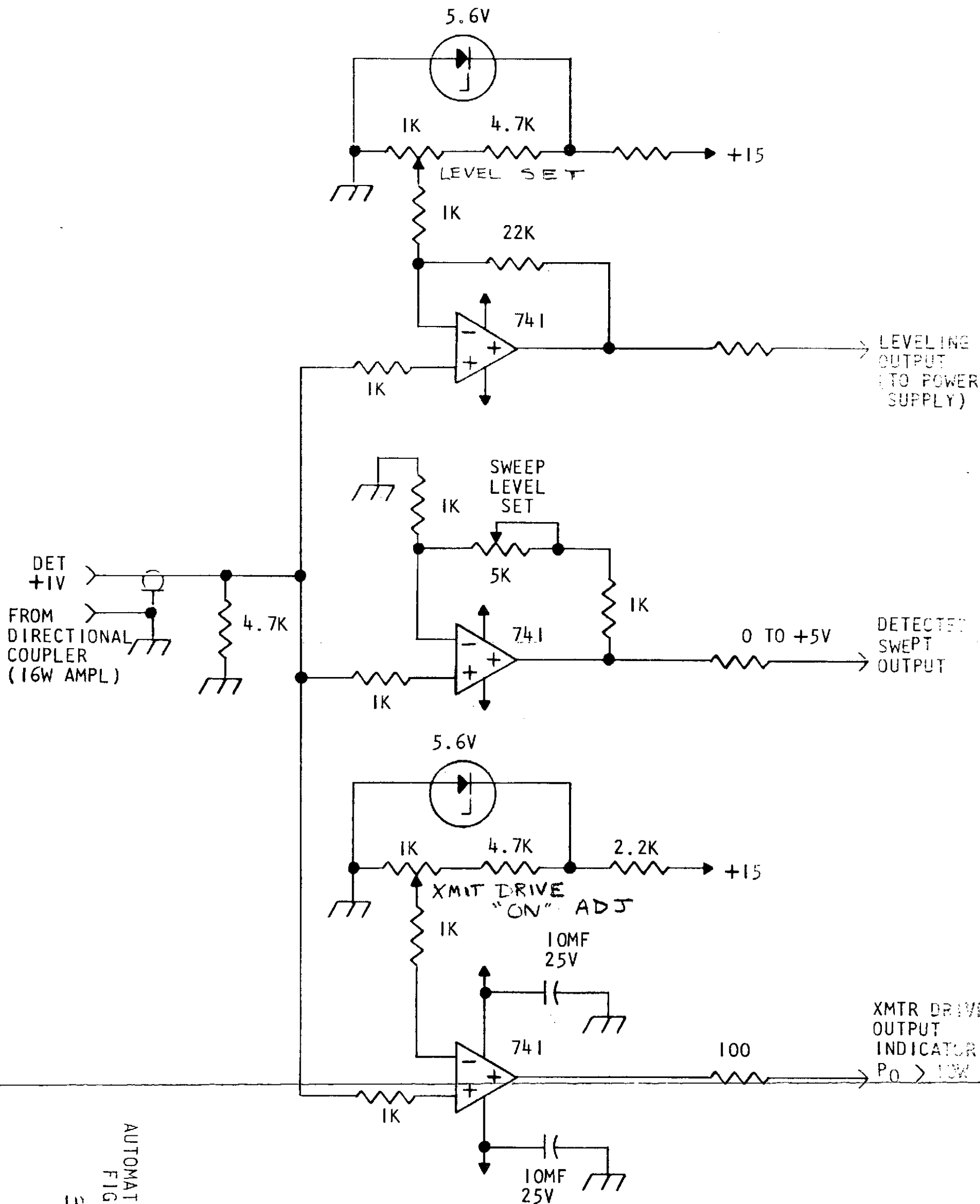
The tentative schematic of the automatic power control is shown in 3.8.2. The sample RF output from the directional coupler is detected and compared with a fixed reference in an operational amplifier. The output of the operational amplifier is used to correct the B+ voltage on the power amplifier such that output power remains constant. The transfer characteristics of the power amplifier indicates a slope of approximately 1 watt per volt.



ANTENNA ELECTRONICS
FIGURE 3.8.1

FOLDOUT FRAME 1

FOLDOUT FRAME 2



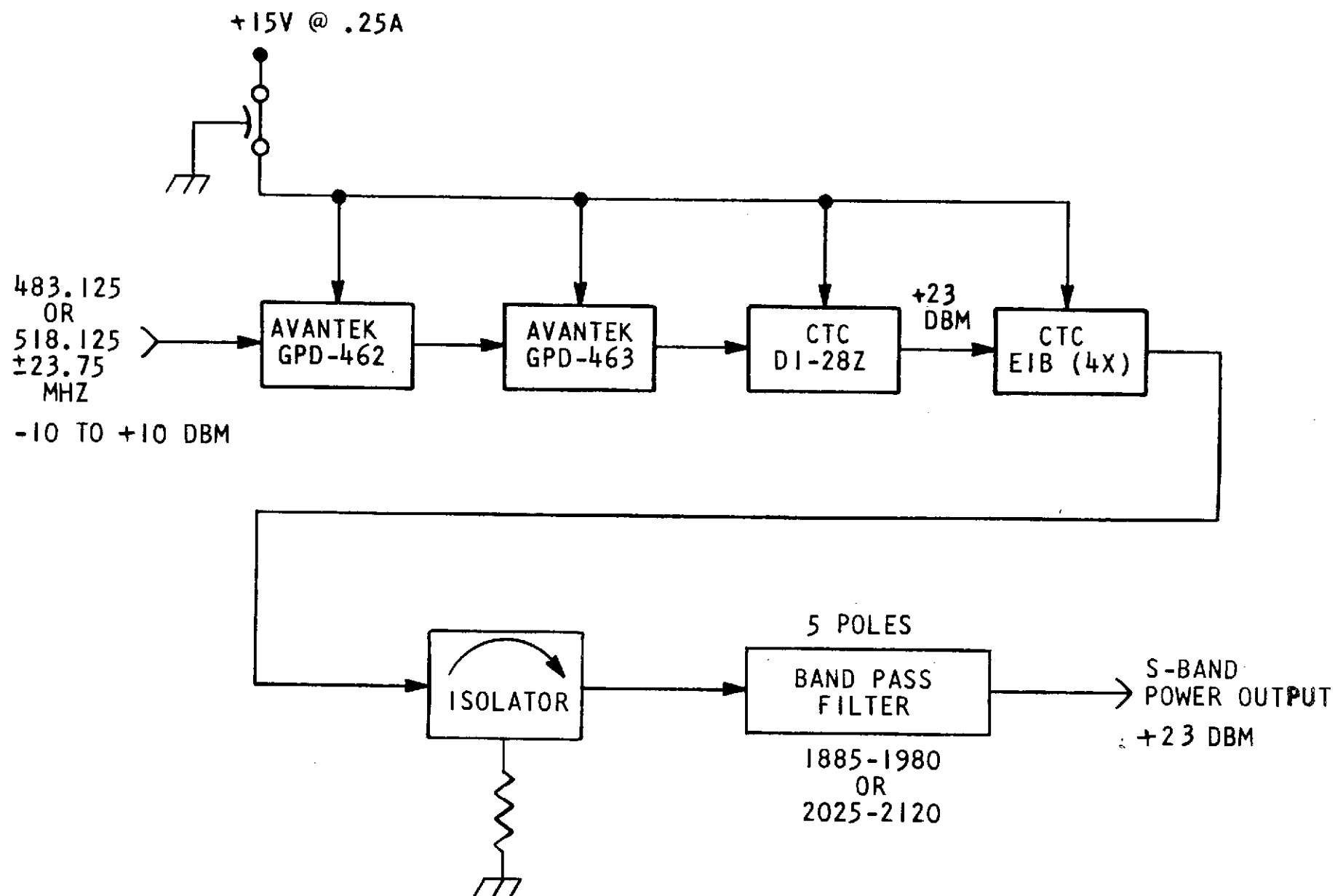
AUTOMATIC POWER CONTROL
FIGURE 3.8.2
3-109

3.8.1.1 Times 4 Multiplier

Figure 3.8.3 is a block diagram of the X4 multiplier. Antenna electronics assembly contains two such units which are packaged in a machined box. Each of these multipliers is identical but differ primarily in alignment. Multiplier No. 1 generates 1885 - 1980 MHz for injecting the verification receiver down converter. The No. 2 multiplier covers 2025 - 2120 MHz and drives S-Band transistor power amplifier.

Two Avantek thin film amplifiers are used to build up the small signal so that a saturated gain characteristic results. This removes IAM and output variations due to drive changes. The second Avantek amplifier is followed by a class "A" amplifier delivering about +23 dBm in the 500 MHz frequency range. This in turn drives a transistor quadrupler thus producing +23 dBm nominal at S-Band. The multiplier is terminated by an isolator to provide proper load and a five pole band pass filter to give more than 60 dB rejection of the 3X and 5X outputs from the multiplier.

The frequency range of the input signal for the multiplier No. 1 from L.O. translator is 471.25 - 495 MHz which on multiplication gives 1885 - 1980 MHz. For multiplier No. 2 the input signal is 506.25 - 530 MHz which on multiplication gives 2025 - 2120 MHz. The output signal level is about +23 dBm which enables to use a large pad at the mixer L.O. input port to produce excellent source impedance.



4X FREQUENCY MULTIPLIER

FIGURE 3.8.3

3.8.1.2 S-Band Amplifier

The S-Band Amplifier contains two modules which are packaged in separate machined RF tight boxes.

1. Driver Amplifier Module
2. Power Amplifier Module

The driver amplifier module consists of two class "C" stages in cascade which raise the 0.25 watts nominal input up to about 6 watts. The power amplifier module consists of two class "C" stages in quadrature which will give 24 watts with 6 watts input.

As indicated in the figure 3.8.1, the power amplifier is terminated by an isolator which is followed by a low pass filter and a directional coupler. The isolator provides protection against open or short circuit load conditions and the low pass filter gives additional harmonic suppression. Three coupled ports of the directional coupler provide sampled outputs for verification receiver down converter, automatic leveling control and frequency translator. Specifications on these items have been agreed to by our vendors and will have maximum insertion loss as follows:

isolator	0.25 dB max
low pass filter	0.20 dB max
directional coupler	0.25 dB max
allowing additional loss	0.30 dB max
for 1 cable	0.30 dB
	<u>1.0</u> dB

For a developed power of 24 watts, this loss would give an output of 21.5 watts. The actual insertion loss measured for the above system is 0.8 dB which indicates that for 16 watts power output, the required output from the power amplifier module will be 17.6 watts.

As the power amplifier is capable of delivering 24 watts and the actual required output is only 17.6 watts, thus we have about 1.0 dB power in reserve which will enable to operate the power transistors at a much lower voltage. This in effect will decrease the dissipation in the devices which will improve the life time. The lower dissipation will also help to minimize the temperature rise in the box.

The 5-pole low pass filter used in the output will provide more than 50 dB of harmonic suppression in the filter itself.

3.8.1.2.1 Driver Amplifier

Figure 3.8 4 represents the schematic of the driver amplifier. It consists of two power transistors in cascade to give 6 watts output with a nominal 0.25 watts input power.

Various devices from different manufacturers have been evaluated. The best choice from gain and power output standpoint is RCA 3003 for the first stage and RCA 2308 (TA8922) for the second stage.

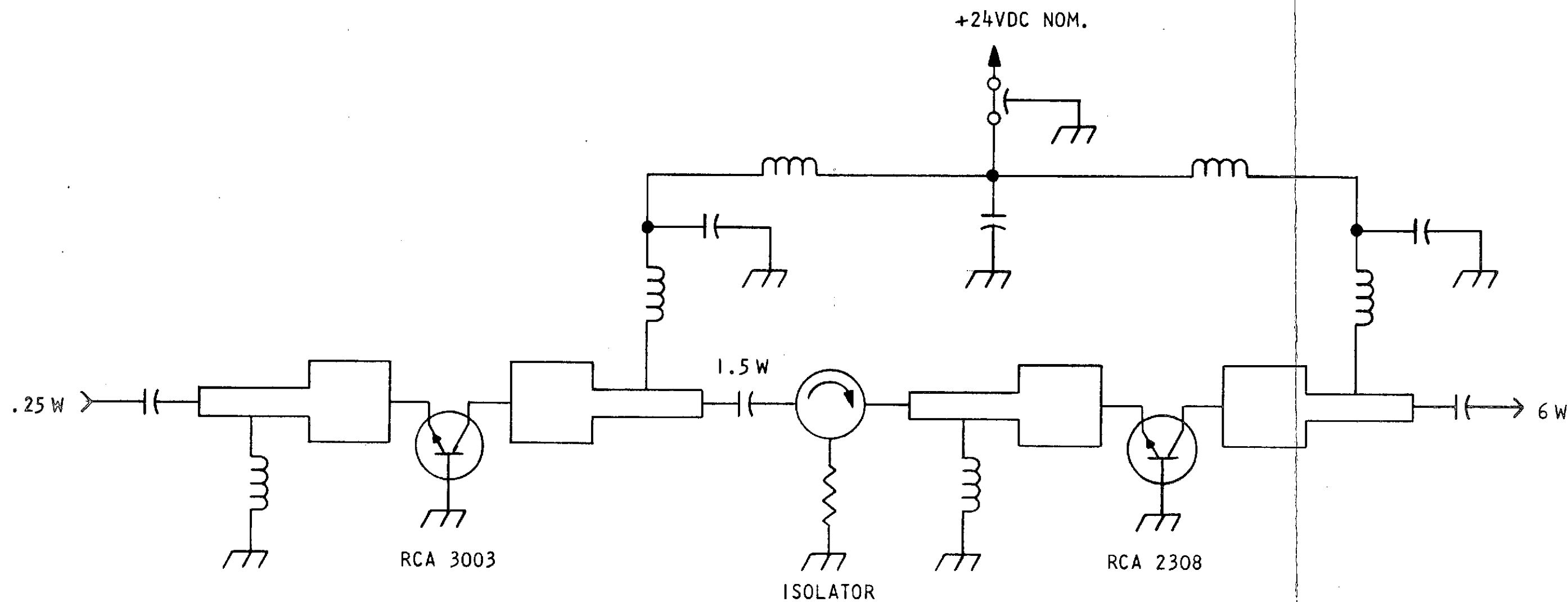
For matching the input and output impedance of each transistor stage, microstrip techniques are employed on 1/32" thick teflon-fiberglass. Small trimming pads are used for optimizing the frequency response (2025 - 2120 MHz) and efficiency. Both stages are operated in class "C" mode.

A regulated +24 volts is used for maximum power gain and output. It is decided to keep B+ fixed so that the driver will always deliver full power into the power amplifier to avoid oscillations due to reduced drive.

The results obtained on the breadboard of RCA 3003 indicate that the device delivers 2.0 watts over the band with 0.25 watts power input. In order to reduce the dissipation it is planned to operate at reduced voltage.

Breadboard for RCA 2308 (TA8922) has been evaluated and 6.0 watts output is obtained over the frequency band with 1.7 watts input power. This output will be sufficient to drive the power amplifier.

The complete driver amplifier is cascaded and it is planned to use an isolator between the two stages to avoid oscillations.



S-BAND
DRIVER AMPLIFIER

FIGURE 3.8.4

The alignment of the complete driver amplifier will be very simple as the circuit constitutes primarily micro-strip matching. No capacitive tuning is used due to high loaded Q for broadband considerations. In case of failure, no additional tuning will be required, only replacement of transistors will be sufficient.

3.8.1.2.2 Power Amplifier

Figure 3.8.5 represents the schematic of the power amplifier which contains two power transistors in quadrature. After complete evaluation, the RCA 2023-12 is selected from the following possible choices.

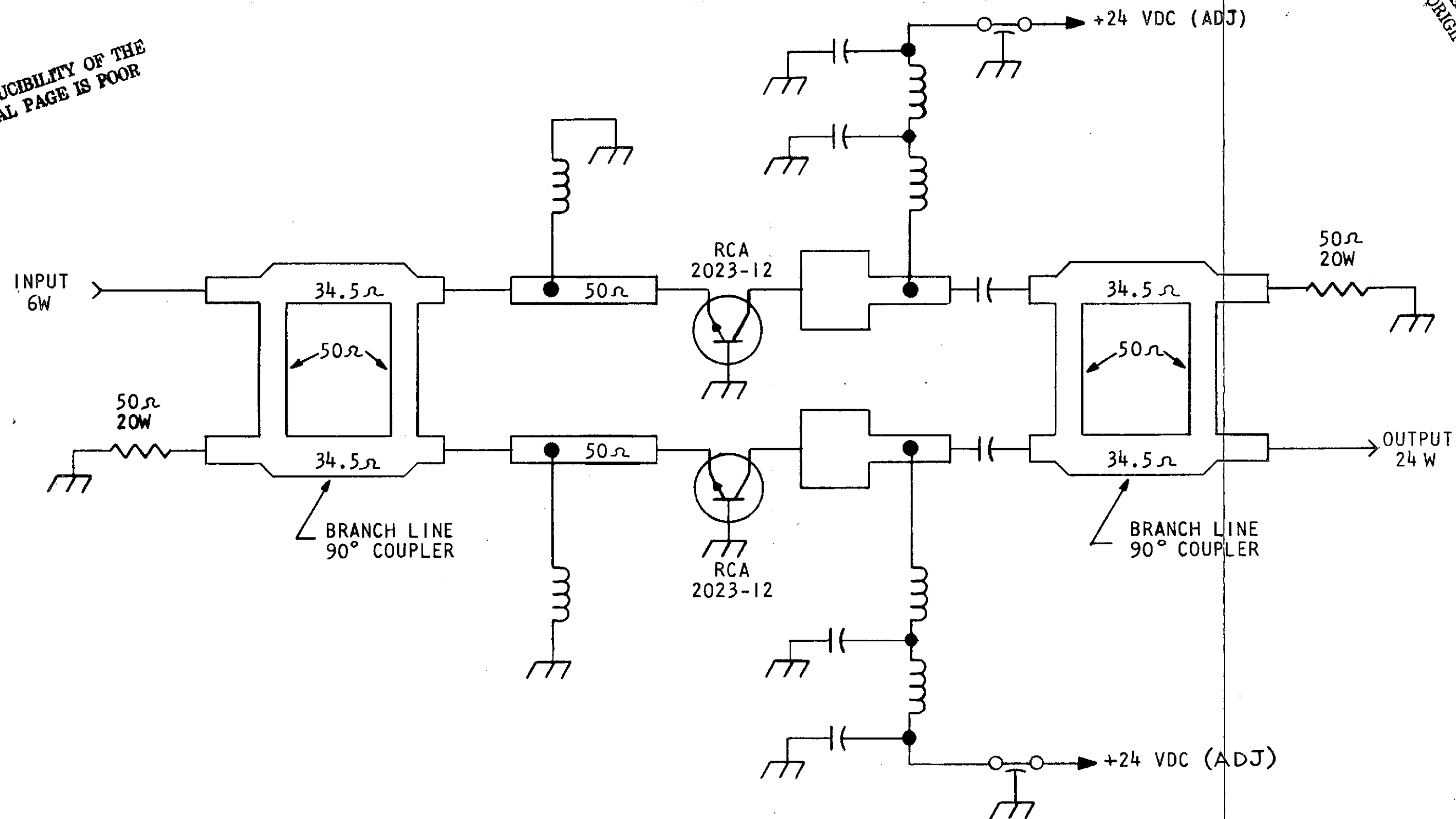
RCA	2023-12	13 W @ 2.2 GHz	9 dB gain
PHI	PH2010C	10 W @ 2.0	6 dB
	PH2020C	20 W @ 2.0	5 dB
	PH2514	14 W @ 2.5	8 dB
TRW	MRA2023-10	10 W @ 2.3	
	MRA2023-14	14 W @ 2.3	8.5 dB
MSC	MSC-1330	18 W @ 2.0	4.5 dB
	MSC-2023-10	10 W @ 2.3	7 dB
CTC	F5-28	6.5W @ 2.1	8 dB
	CD2153	13 W @ 2.1	7 dB

The input power from the driver amplifier is split by a 3 dB, 90° branch line coupler to drive each transistor. The output from each transistor is combined by another 3 dB, 90° branch line coupler. The input and output impedances of each transistor are matched by utilizing microstrip techniques on a 1/32" thick teflon-fiberglass. No capacitive tuning is employed to minimize loaded Q for bandwidth considerations.

The complete power amplifier will be printed on a 1/32" thick teflon-fiberglass board including the input/output couplers. The results obtained on couplers show typically 1L = 0.2 dB, split = ±0.1 dB and isolation > 25 dB. The bread-board for the complete amplifier is built using RCA 2032-12 and 24 watts is obtained over the frequency band with 5 watts input. The alignment of the complete power amplifier is simple as the circuit constitutes only microstrip matching. In case

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24 WATT S-BAND
POWER AMPLIFIER

FIGURE 3.8.5

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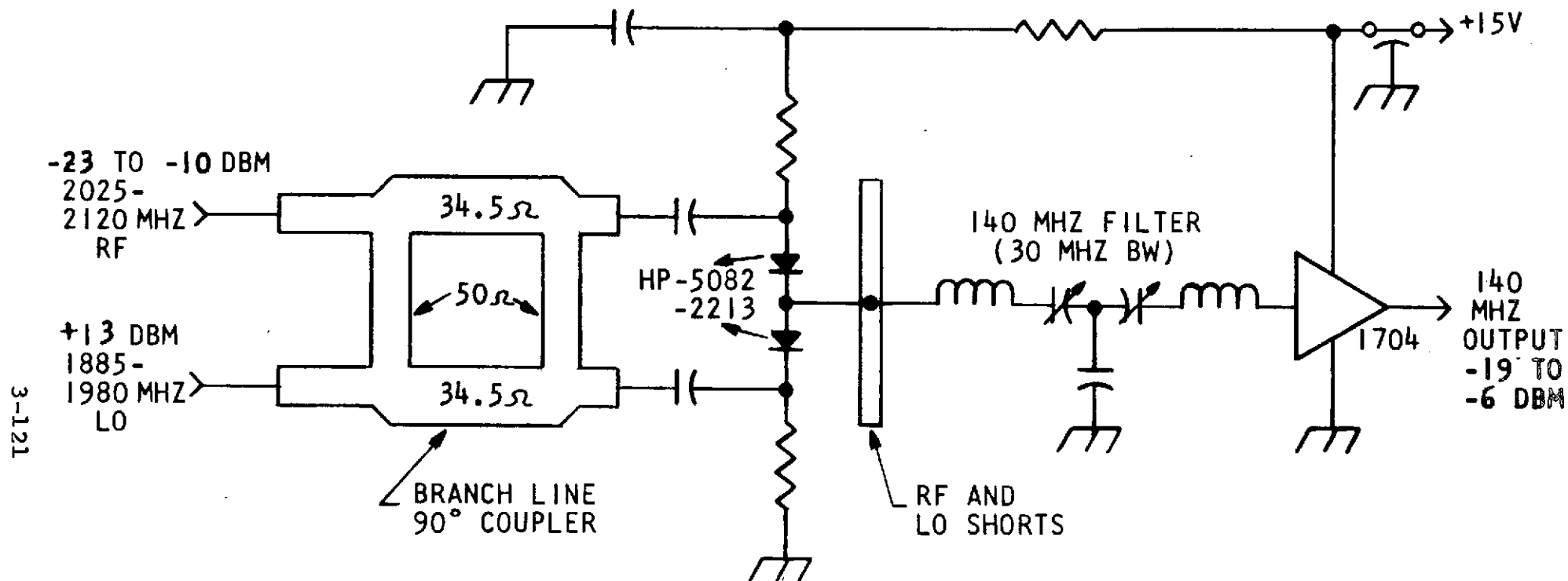
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of failure, replacement of the transistor will be sufficient and no additional tuning will be required.

3.8.1.3 Verification Receiver Down Converter

Figure 3.8.6 represents the schematic for the verification receiver down converter. The No. 1 times 4 multiplier develops the +13 dBm, L.O. signal required to saturate the HP-5082-2213 mixer diodes. To date several of these branch line couplers have been fabricated. More than 30 dB isolation between the RF and L.O. ports is obtained. Open circuited $\lambda/4$ lines are used as L.O. and RF shorts. The complete circuit will be fabricated on a 1/16" thick teflon-fiberglass utilizing micro-strip techniques and will be packaged in a small machined box as a complete subassembly.

The breadboard for the verification receiver down converter has been evaluated and released for final artwork. The mixer has a conversion loss of 8 dB over 30 MHz bandwidth. The spurs are greater than 60 dB down.

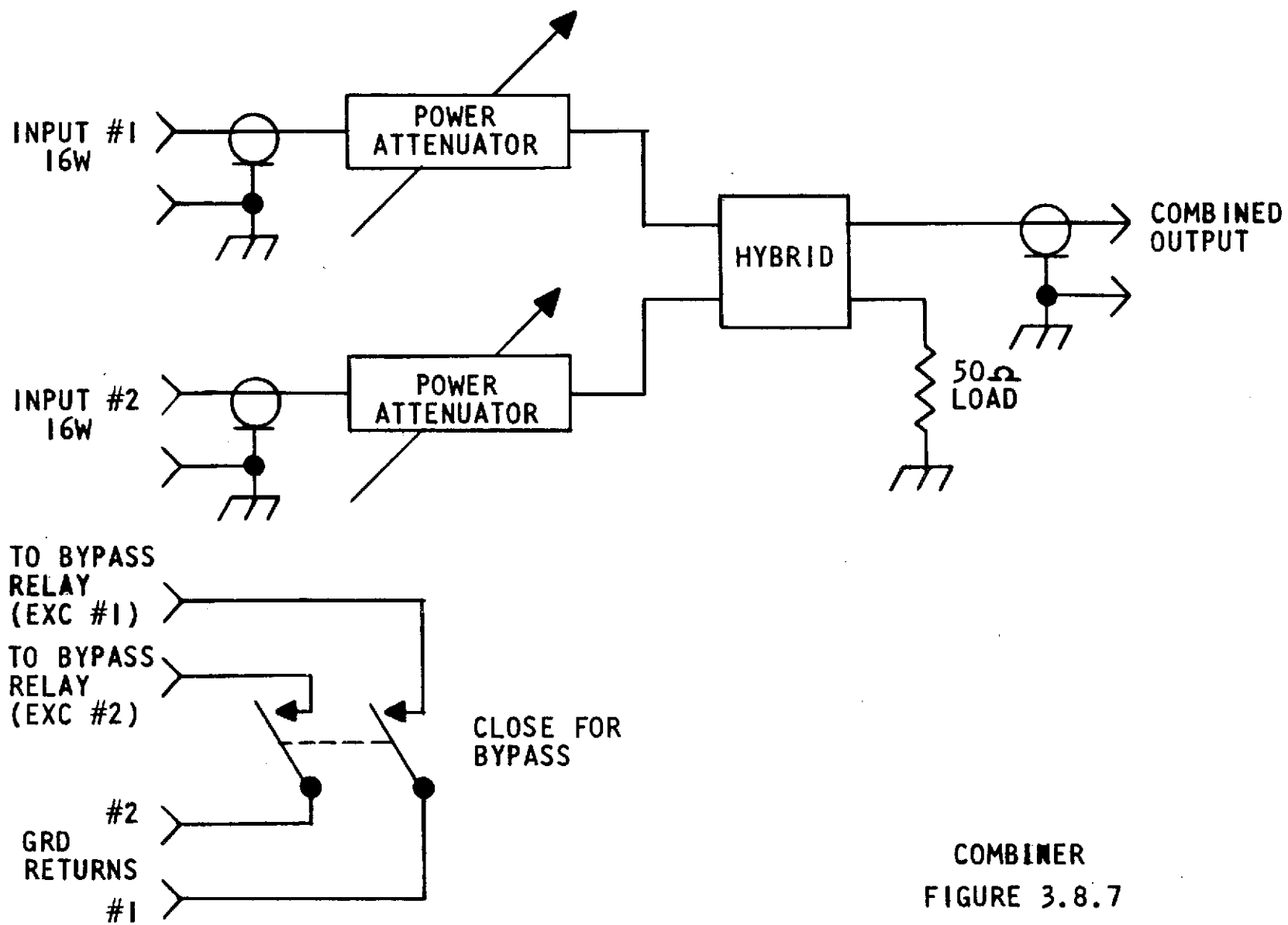


VERIFICATION RECEIVER
DOWN CONVERTER

FIGURE 3.8.6

3.8.2 Output Combiner

The output combiner is mounted on a 5-1/4 inch front panel and is configured as shown in Figure 3.8.7. Inputs and outputs are located on the rear of the unit and a switch to bypass the exciter output around the combiner is provided on the front panel. Also located on the front panel are two micrometer screw adjustment knobs for the power attenuators (Merrimac AU-10A) on the input from each exciter. The attenuators feed into a hybrid combiner (Merrimac QHM-2-3G) having an output to feed the power amplifier. A 20 watt 50 ohm termination (Engleman Microwave T515-4) is connected to the fourth port of the hybrid and will dissipate half the power from each attenuator. A relay to switch the exciter output around the combiner is located in the output of the exciter amplifier drawer.



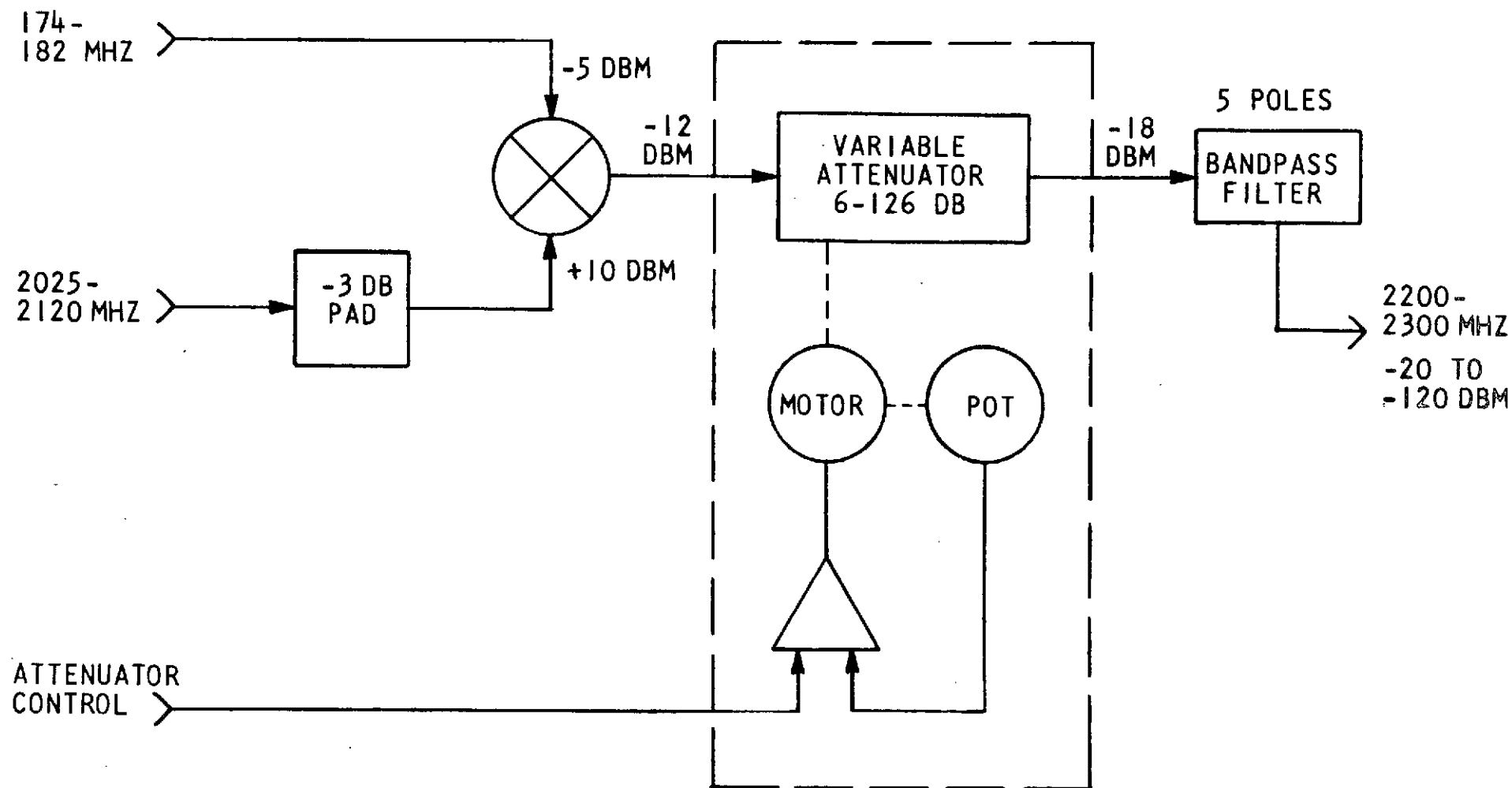
COMBINER
FIGURE 3.8.7

3.8.3 Frequency Translator

Figure 3.8.8. is a diagram showing the content of the translator assembly. A Merrimac type SMM-1-2000 mixer is used to upconvert the transmit signal (2025-2120 MHz) to the receive band of 2200-2300 MHz. A 3 dB pad on the L.O. input is to provide better VSWR characteristics. A servo controlled attenuator assembly, previously designed at RF, follows the mixer and will give the required setting accuracy of ± 1 dB at the output. The filter used in the output has an in-band flatness of $\pm .1$ dB. Also tests on the mixer show that a flatness of better than .1 dB can be expected. No difficulty is expected in meeting the required setting accuracy specification.

The translator is entirely mounted on a single panel which can be removed from its dip-brazed box by removing 14 screws and lifting the assembly up and out, providing full access to all parts. The case and panel are white gloss enamel with black marking. The translator is designed to be pressurized and has a gauge to measure the pressure (full scale reading is 5 psi), a Schraeder valve for charging and a pressure relief/purge valve for purging the unit while charging plus preventing the pressure from going above about 2.3 psi (see Fig. 3.8.9).

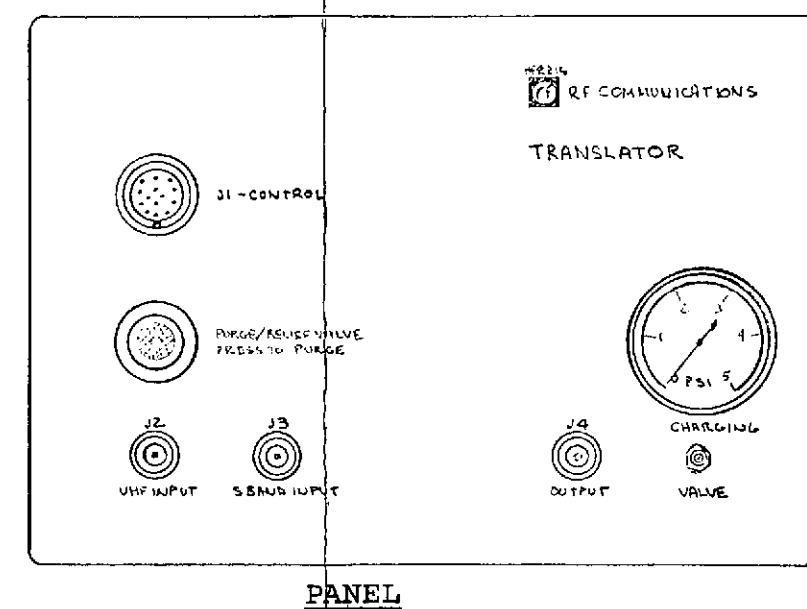
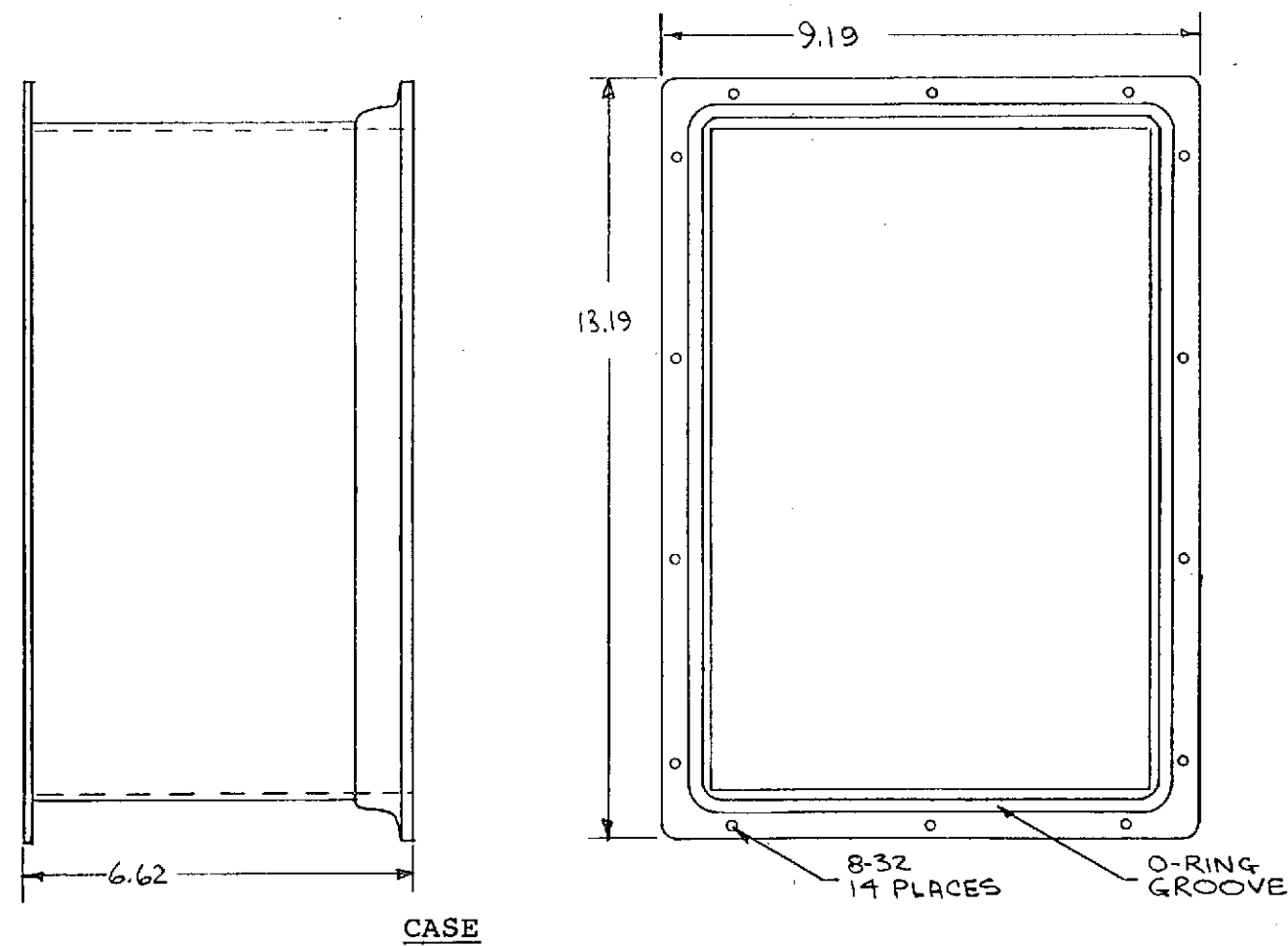
The control lines entering the translator pass thru a sealed 35 pin connector, a filter box and then are coupled through another connector which is part of the servo drive assembly, thus enabling the servo drive to be removed and/or replaced without unsoldering any connections. All RF coax cables are .141 teflon dielectric rigid coax. The coax connector on the outputs and inputs are type N and all others are SMA.



TRANSLATOR
FIGURE 3.8.8

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TRANSLATOR
FIGURE 3.8.9

3-126

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FOLDOUT FRAME 2

3.8.4 Antenna Equipment Mechanical Design

The antenna electronics assembly, which contains the majority of the antenna equipment, is contained behind a 7 x 19 inch rack panel. It is slide mounted, tiltable in 45° increments up and down and has front panel handles with which to maneuver it. See Figure 3.8.10 for layout.

The units in this chassis are as follows:

1. X4 Multiplier (518 MHz to 2072 MHz)
2. Driver Amplifier
3. Output Amplifier
4. Blower
5. Low Pass Filter
6. Output Directional Coupler
7. Combiner Bypass relay
8. Verification Receiver Downconverter
9. X4 Multiplier for Downconverter
10. Relay for selecting downconverter input sample
11. Interstage bandpass filters and isolators.
12. Printed Circuit Card

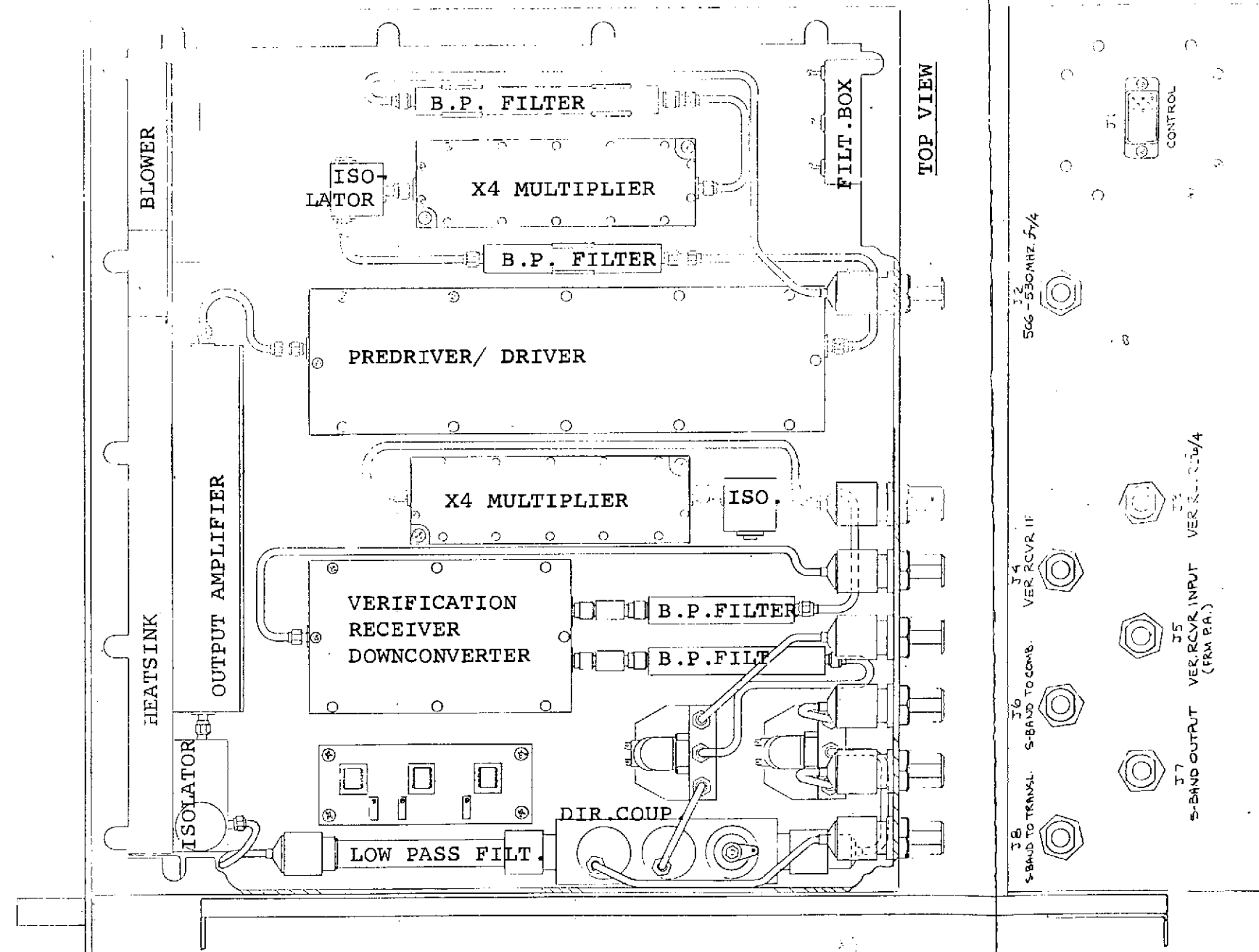
Most of the circuitry is mounted in the bottom of a 5 inch deep chassis with the exception of the output amplifier module and output isolator which are mounted on a heatsink and bracket with a Rotron Biscuit blower; the amplifier unit (blower, heatsink, amplifier and isolator) is mounted to the bottom of the chassis and is easily removable so that it may be operated on a bench for test and alignment. The air, after passing thru the heatsink, passes out the side of the chassis thru a honeycomb filter, thus providing RFI integrity of the chassis.

The blower is operated on 117 VAC and is running only when the amplifiers are on. The cover of the chassis is held on by 1/4 turn fasteners and has RFI gasketing to be RFI tight. Air intake is thru a honeycomb filter located in the corner of the cover opposite the blower so that fresh air is pulled across all the amplifiers and multipliers to keep them cool.

The chassis is 16.62 inches wide by 15 inches deep by 5 inches high. It is fabricated of 3/32 inch thick aluminum with iridite for corrosion resistance. The slides are cadmium plated steel with ball bearings. They withdraw out 21 inches, therefore, as the chassis is only 15 inches deep, there is 6 inches clearance behind the chassis for cables to swing when tilting the chassis.

All the control wires entering the chassis pass thru a connector and filter box. The majority of these wires are the B+ voltages for the amplifiers and multipliers as the power supply is located on the exciter Antenna Control Panel.

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S-BAND AMPLIFIER
FIGURE 3.8.10
3-129

FOLDOUT FRAME

3.8.5 Thermal Analysis

The S-Band power amplifier thermal analysis is based on the following assumptions.

1. Continuous operation at 70°C ambient.
2. The dissipating power transistors are mounted direct to the box housing with silicone grease between the interface. The temperature gradient between the transistor flange and housing is assumed negligible.
3. The box housing of each module is bolted to a plate (heat sink) with silicone grease between the interface. The rise in junction temperature due to this interface is approximated by $0.446 P_{DISS}$ where P_{DISS} = total power dissipation, watts.
4. The total heat is transferred to mounting surface by conduction only.
5. The housing is isothermal.

The computations for power dissipations are based upon data taken from breadboards for different transistors.

Freq. MHz	RF P _{out} Watts	Input DC Power			Total Input DC Power, Watts	Dissipation Watts
		RCA 3003 Watts	RCA 2308 Watts	RCA 2023-12 Watts		
2025	24	$0.30 \times 24 = 7.20$	$0.9 \times 24 = 21.6$	$3.1 \times 24 = 74.4$	103.2	79.2
2072	24	$0.33 \times 24 = 7.92$	$0.8 \times 24 = 19.2$	$3.1 \times 24 = 74.4$	101.52	77.52
2120	24	$0.31 \times 24 = 7.44$	$0.8 \times 24 = 19.2$	$3.0 \times 24 = 72.0$	98.64	74.64

The worst case junction temperature for each transistor is computed applying the following equation:

$$\text{Junction Temp.} = 70 + 0.446 P_{DISS} + R_{TH} P_{DISS}$$

R_{TH} = Thermal resistance, °C/W

P_{DISS} = Total power dissipation, watts

Freq. MHz	Junction Temp (°C)		
	RCA 3003	RCA 2308	RCA 2023-12
2025	150.3	163.0	177.8
2072	161.5	150.0	177.8
2120	154.5	152.78	173.1

The thermal resistances of different transistors are used as supplied by the manufacturer.

	R_{TH}
RCA 3003	15 °C/W
RCA 2308	5 °C/W
RCA 2023-12	1.5 °C/W

All the junction temperatures are well below maximum operating temperature of 200°C specified by the vendor. For additional reliability it is planned to use fins and fan to cool power amplifier module.

The breadboard for complete amplifier has been tested and is determined that the currents in the different transistors are running much lower than specified in the above analysis. This is primarily due to the reduced insertion loss of isolator, directional coupler, low pass filter, etc. Therefore it is concluded that junction temperatures of different transistors will be much lower in the actual overall system.

4.0 SYSTEM ANALYSIS

4.1 Phase Noise

4.1.1 Analysis of the Requirement

The phase noise requirement for the exciter is given in paragraph 4.1.4 of the specification and states:

Phase jitter at any selected exciter frequency shall be less than 1.0° rms during the fixed frequency mode of operation.

An expression for an RF signal perturbed by phase noise is

$$v(t) = A \cos [w_0 t + \phi(t)]$$

where $\phi(t)$ is a time function which represents the phase noise. Phase noise density $S_\phi(f)$ as defined by Cutter and Searle (ref. 1) is the two-sided power spectral density of $\phi(t)$. The auto-correlation functions of $\phi(t)$ and $S_\phi(f)$ form a Fourier transform pair

$$R_{\phi\phi}(\tau) = \int_{-\infty}^{\infty} S_\phi(f) e^{j2\pi f\tau} df$$

and the variance of $\phi(t)$ is

$$\overline{\phi^2(t)} = R_{\phi\phi}(0) = \int_{-\infty}^{\infty} S_\phi(f) df$$

The power spectral density function is symmetrical, so that

$$\overline{\phi^2(t)} = 2 \int_0^{\infty} S_\phi(f) df$$

Ref. 1 - L. S. Cutter and C. L. Searle, "Some Aspects of the Theory and Measurement of Frequency Fluctuations in Frequency Standards", Proc. IEEE, p. 136, February 1966.

$S_{\phi}(f)$ can be measured by passing the signal $v(t)$ through a phase detector and examining the output with a wave analyzer and an RMS Voltmeter. With proper calibration, the result has the dimensions radians per root Hz, and can be converted to the power spectral density $S_{\phi}(f)$ by squaring. In practice, the phase detector generally has a sinusoidal response characteristic, which simplifies the calibration procedure as follows:

Let the phase detector output be represented by

$$e(t) = K \sin \phi(t)$$

For practical signals, $\phi(t) \ll 1$ radian, so that a good approximation for the phase detector output is

$$e(t) = K\phi(t)$$

so that K can be identified as the phase detector constant in volts per radian. The value of K is easily found by observing the peak amplitude of the detector output when the inputs differ in frequency by a small amount. Consequently, the wave analyzer can be calibrated to read directly in dB below one radian by setting the reference level on the beat frequency.

Measurement procedures based on the phase detector method fold the phase noise into a one-sided spectrum. Therefore, integrated phase noise is obtained by squaring the measured values and integrating over positive frequencies only. The corresponding double-sided values of $S_{\phi}(f)$ are obtained by dividing the measured values by 2 or $\sqrt{2}$, depending on whether the noise voltage is assumed to be correlated in the upper and lower sidebands; the factor 2 is commonly used for close-in noise. It can be shown (see for example, ref. 2) that $\overline{\phi^2(t)}$ is the total sideband noise to signal power ratio for a phase modulated signal.

4.1.2 Phase Noise Model of the Exciter

For the purposes of phase noise analysis, the exciter can be modeled as in Figure 4.1.1. The input is supplied by a 5 MHz standard, and the synthesizer is assumed to operate at about mid-band (175 MHz output). The synthesizer output is sidestepped in mixer M1. A final X4 multiplier raises the output of M1 to S-Band (2080 MHz).

Figure 4.1.2 shows the results of phase noise measurements made on the MFR synthesizer which will be used in the exciter. Figure 4.1.3 is a diagram of the test set-up. The synthesizer RMS phase noise is obtained by numerical integration of the phase noise power spectral density curves of figure 4.1.2.

The one-sided spectrum of figure 4.1.2 is approximated with straight-line segments.

For each straight-line segment, the power density function has the form

$$S_{\phi}(f) = K f^a$$

and the integrated phase noise is given by

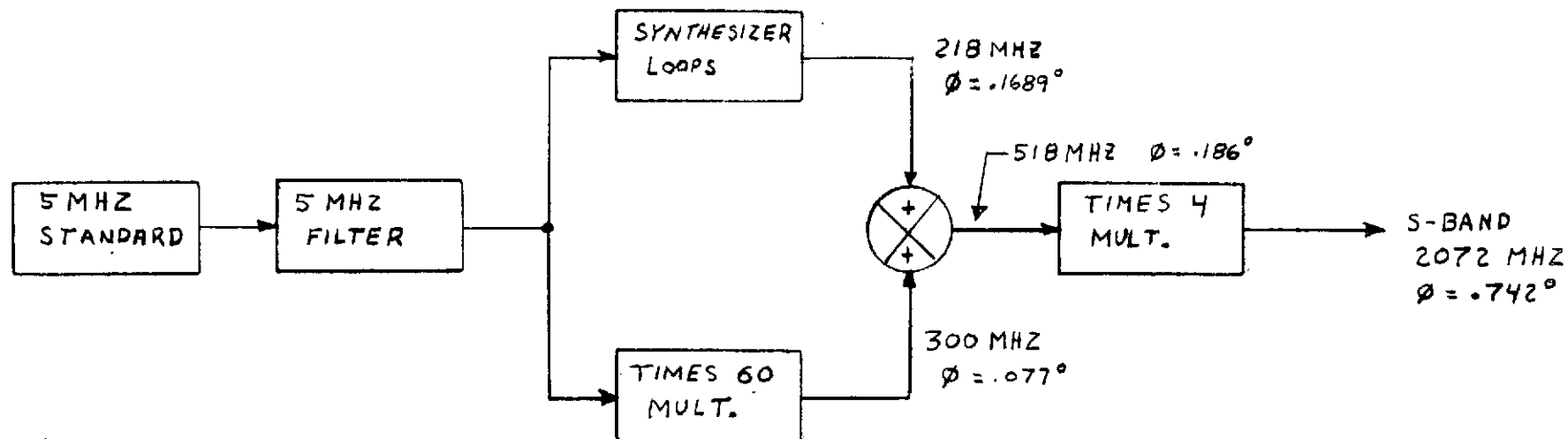
$$\begin{aligned} \overline{\phi^2}(t) &= \int_0^{\infty} S_{\phi}(f) df = \frac{K}{a+1} f^{a+1} \Big|_0^{\infty} & a \neq -1 \\ &= K \log f & a = -1 \end{aligned}$$

Evaluation of K and a for each straight-line segment is illustrated by the following example for the segment: $10 \leq f \leq 100$ Hz.

$$10 \left[\log K + a \log 10 \right] = -73.5 \text{ dB}$$

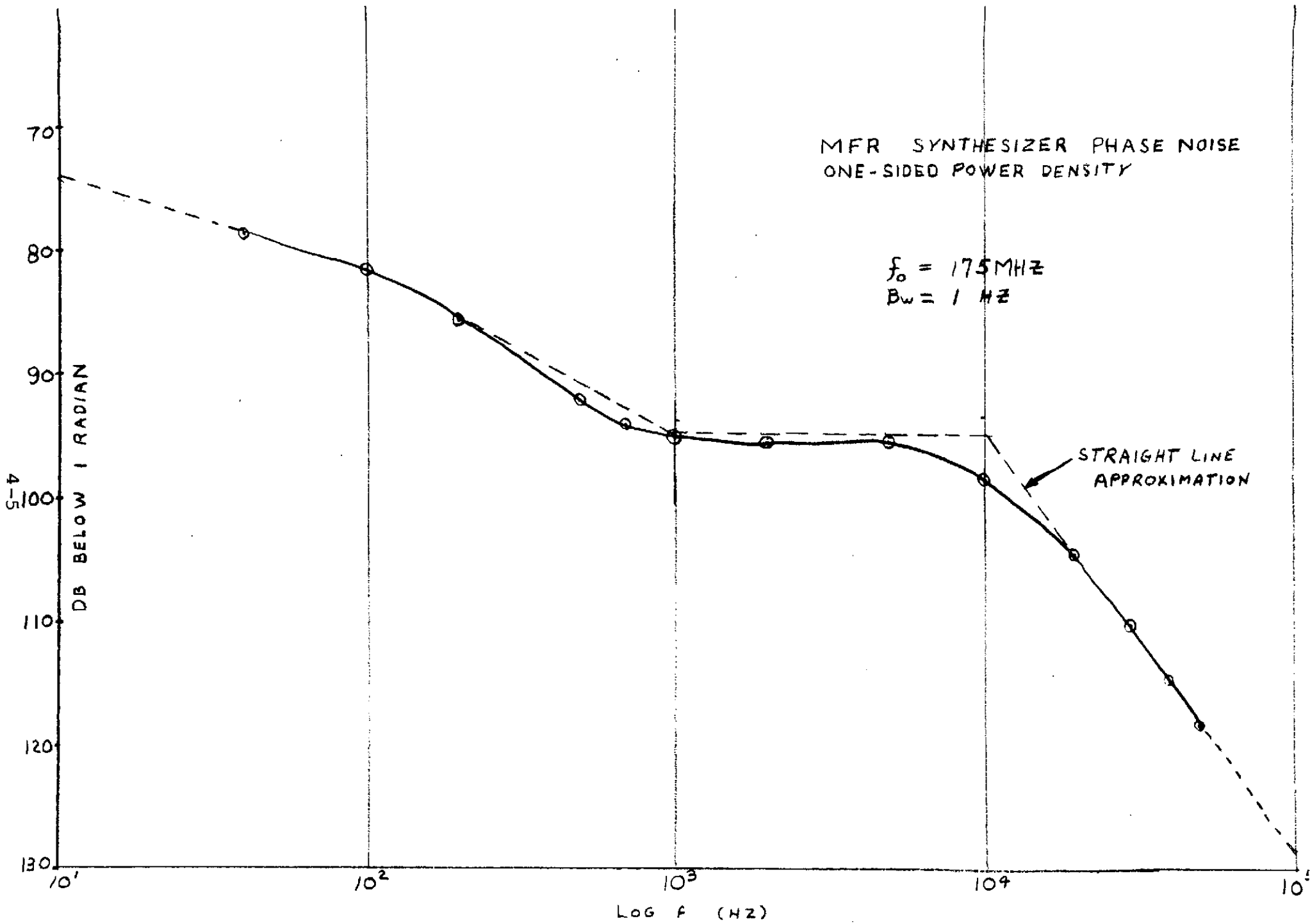
$$10 \left[\log K + a \log 100 \right] = -81.5 \text{ dB}$$

Ref. 2 - D. G. Meyer, "An Ultra Low Noise Direct Frequency Synthesizer", John Fluke Manufacturing Co., July 1970



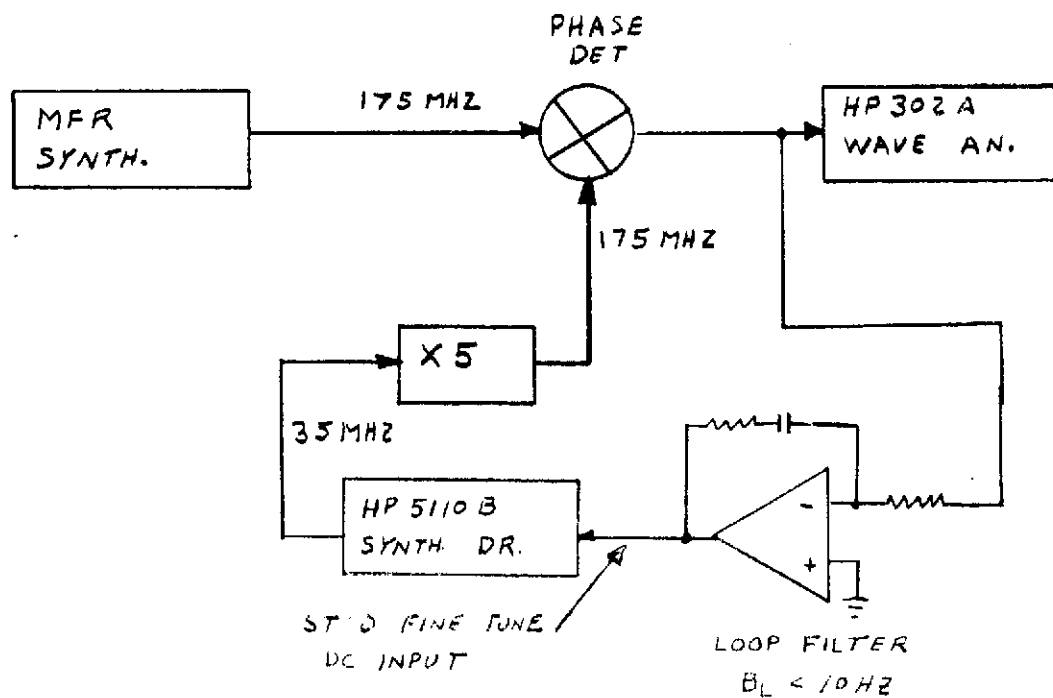
S-BAND EXCITER PHASE NOISE MODEL

FIGURE 4.1.1



OFFSET FREQUENCY

FIGURE 4.1.2



MFR SYNTHESIZER PHASE NOISE MEASUREMENT
TEST SET UP
FIGURE 4.1.3

Solving these equations for K and a leads to

$$S_{\phi}(f) = 2.82 \times 10^{-7} f^{-.8}$$

To evaluate the integrated phase noise in the interval 1 to 100 Hz (assuming the noise maintains the same slope below 10Hz),

$$\overline{\phi^2(t)} = \frac{2.82 \times 10^{-7}}{.2} f^{.2} \bigg]_1^{100} = 2.14 \times 10^{-6} \text{ rad}^2$$

For $100 \leq f \leq 1000\text{Hz}$

$$S_{\phi}(f) = 1.12 \times 10^{-6} f^{1.35}$$

and

$$\overline{\phi^2(t)} = 0.352 \times 10^{-6} \text{ Rad}^2$$

For $1000 \leq f \leq 10,000 \text{ Hz}$,

$$S_{\phi}(f) = 4.47 \times 10^{-10}$$

and

$$\overline{\phi^2(t)} = 4.425 \times 10^{-6} \text{ Rad}^2$$

For $10,000 \leq f \leq 100,000 \text{ Hz}$,

$$S_{\phi}(f) = 4.425 \times 10^{-4} f^{-3.5}$$

and

$$\overline{\phi^2(t)} = 1.77 \times 10^{-6} \text{ Rad}^2$$

The total mean squared phase noise is taken as the sum of the above, i.e., $8.687 \times 10^{-6} \text{ Rad}^2$. The RMS phase jitter is 2.947×10^{-3} radians or 0.1689 degrees.

To obtain the total phase noise at the mixer output the phase noise of the 300 MHz fixed frequency must be obtained. The phase noise spectral density is plotted in figure 4.1.4. This curve was obtained by scaling the Frequency standard specification as follows:

1. Add 35.6 dB for times 60 multiplication
2. Add 6.0dB for converting SSB noise to a one sided spectrum
Add 41.6dB Total

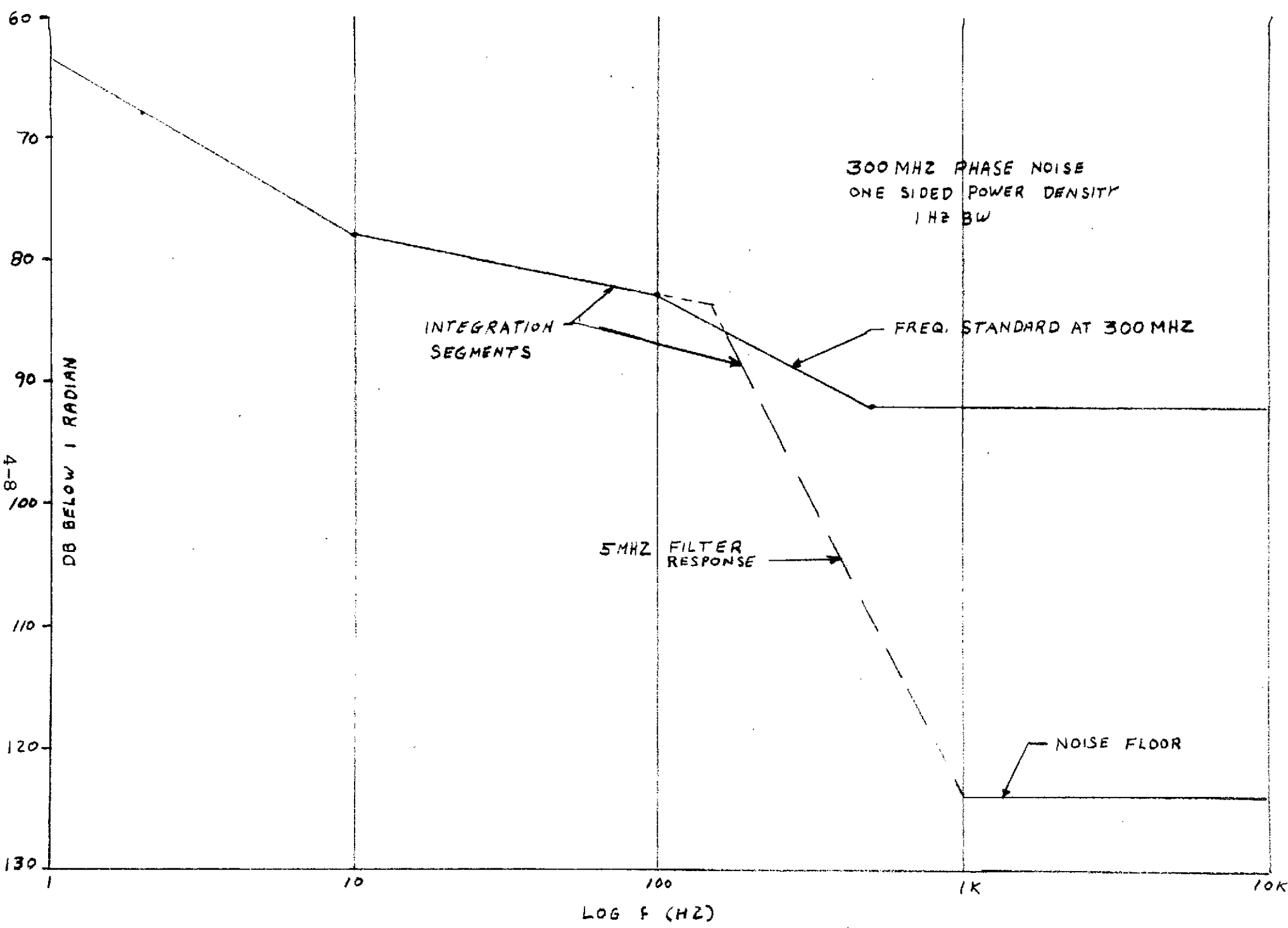


FIGURE 4.1.4

The output of the frequency standard is filtered in a three section narrowband crystal filter. This filter has a 3dB bandwidth of 400Hz and a 40 dB bandwidth of 3 KHz. The effect of the filter on the phase noise spectrum is shown in figure 4.1.4. An absolute noise floor of -124 dB per Hz was assumed at 300MHz. This corresponds to -160 dB per HZ at 5 MHz or in other words a 160 dB signal to noise ratio per HZ bandwidth at the first multiplier input.

To obtain the mean square phase noise, the curve is approximated with straight line segments and integrated following the same procedure that was used to obtain the synthesizer noise. The following values apply.

$$1 \leq f \leq 10 \text{ Hz}$$

$$S_{\phi}(f) = 5.0 \times 10^{-7} \frac{-1.5}{f}$$

$$\overline{\phi^2(t)} = 6.84 \times 10^{-7} \text{ Rad}^2$$

$$10 \leq f \leq 200 \text{ Hz}$$

$$S_{\phi}(f) = 5.5 \times 10^{-8} \frac{-1.54}{f}$$

$$\overline{\phi^2(t)} = 10.28 \times 10^{-7} \text{ Rad}^2$$

$$200 \leq f \leq 1000 \text{ Hz}$$

$$S_{\phi}(f) = 1.48 \times 10^{-2} \frac{-4.86}{f}$$

$$\overline{\phi^2(t)} = .506 \times 10^{-7} \text{ Rad}^2$$

$$10^3 \leq f \leq 10^5 \text{ Hz}$$

$$S_{\phi}(f) = 4 \times 10^{-13}$$

$$\overline{\phi^2(t)} = .396 \times 10^{-7} \text{ Rad}^2$$

The total mean square phase noise is the sum of the above, i.e. $1.802 \times 10^{-6} \text{ Rad}^2$. The RMS phase jitter is 1.34×10^{-3} radians or 0.077 degrees.

The total phase noise at the mixer output is the RMS sum of the synthesizer and 300 MHz noise or:

$$\begin{aligned}\overline{\phi^2(t)} &= 8.687 \times 10^{-6} + 1.802 \times 10^{-6} \\ &= 10.489 \times 10^{-6} \text{ Rad}^2\end{aligned}$$

$$\sqrt{\overline{\phi^2(t)}} = 3.239 \times 10^{-3} \text{ Rad}$$

or 0.186 degrees

The predicted S-Band phase jitter is four times this, or 0.742 degrees.

4.2 Spurious Response Analysis

The spurious response requirements of specification paragraph 4.1.5 are divided into three separate areas

- 1) In-band/Out-of-band spurious 60 dB
- 2) 2200-2300 MHz band, less than -135 dBm (-177 dB)
- 3) Harmonics 50 dB

Of these requirements, the 50 dB harmonic rejection is the easiest to achieve. A low pass filter follows the solid-state S-Band amplifier (described in Section 3.8) is used to assure this rejection.

The in-band spurious response of 60 dB is a more difficult, though achievable, task. This level, referred back to the 506-530 MHz output of the exciter, before X4 multiplication, is 72 dB. This is due to the well known relationship that when frequency multiplication is performed, spurious signals are increased by $20 \log N$, where N is the integer of multiplication. In this instance $N = 4$, and 12 dB is the degradation experienced. In-band spurious signals can originate from two different sources. The first source is due to the phase lock loop reference frequency causing PM sidebands on the VCO of the synthesizer. As discussed in Section 3.2.3, these spurious sidebands are typically 80 dB or more below the synthesized signal in the MFR production receivers. The second source of spurious sidebands are those created in the multiplying and mixing operations which generate the reference frequencies. The solution to this source of spurious signals is 1) the careful selection of mixing frequencies to avoid obvious low order in-band "spurs" which cannot be filtered at the mixer

output, 2) the use of multipole band pass filters (BPF) with ultimate skirt rejections in excess of 100 dB, 3) the exclusive use of double-balanced mixers with this inherent spur canceling capabilities. These techniques have been applied in the design presented herein and, when implemented properly, will yield a synthesizer spurious level better than 80 dB. In the approach chosen, Figure 3.2.1, the coarse synthesizer loop provides additional filtering of spurious responses generated in translating the intermediate and fine loops up to VHF.

The final mix, translating the synthesizer 206.25 to 230 MHz signal to 506.25 to 530 MHz by mixing with 300 MHz is the most critical mix in the system. Letting the 300 MHz signal be the local oscillator (L) and the 206.25 to 230 MHz signal be the linear signal (R) the worst case spurious and their levels are tabulated in Table 4.2.1.

From the table it can be seen that to meet the spurious specification the full characteristics of high level double balanced mixer must be realized. For this reason, the linear input to the mixer is filtered just prior to mixing to insure that there are no harmonics on the input signal. The level of the linear signal is also kept low (-10 dBm) to reduce the amount of harmonic generation in the mixer. A level control is used in the L.O. signal path to optimize the mixer performance.

The most difficult requirement to meet is the -177 dB spurious response in the 2200 to 2300 MHz band. Any spurious output between 80 and 275 MHz removed fall in the 2200-2300 MHz

TABLE 4.2.1

S-BAND FINAL MIXER SPURIOUS RESPONSE

L = 300 MHz +13 dBm

R = 206.25 - 230 MHz -10 dBm

I = 506.25 - 530 MHz -17 dBm

Spur	Mixer Output Level in dB		Spurious Freq. Band (MHz)	Filter Requirements	
	Below Desired	Spec		Att (dB)	Freq. (Note 1)
4L - 3R	>90	>80	581.25 - 510		
5R - 2L	>90	>80	431.25 - 550		
4R - L	>90	>80	525 - 620	110	610 - 620
3L - 2R	75	78	487.5 - 440	112	440 - 450
5L - 5R	>90	>80	468.75 - 350	110	350 - 433.3
7R - 3L	>90	>80	543.75 - 710	110	593.3 - 710
5L - 4R	>90	>80	675 - 580	110	604 - 675
6R - 3L	>90	>80	480 - 337.5	110	337.5 - 444
L	4	1	300	188	300
2L	31	9	600	180	600
2R	86	>80	412.5 - 460	110	412.5 - 440
3R	87	>80	618.75 - 690	110	618.75 - 683.75
IMAGE	0	0	93.75 - 70	72	

NOTES:

1. These spurious signals fall in the 2200 - 2300 MHz band after multiplication.

band ($2025 + 275 = 2300$; $2120 + 80 = 2200$ MHz). From Table 4.2.1 it can be seen that several spurious responses fall in this category. The worst case spur is the 300 MHz L.O. feed-through, which looks like a 206.25 to 230 MHz sideband. Since this signal is multiplied by four, these spurious sidebands must be 189 dB down. To achieve this, two six-pole filters are used after this mix. One filter is located immediately after the mixer and the other is located at the end of the cable running to the antenna and preceding the times four multiplier.

4.3 Time Delay Analysis

The time delays in the exciter from the PM modulation input to the 2025 to 2120 MHz output are shown in Figure 4.3.1.

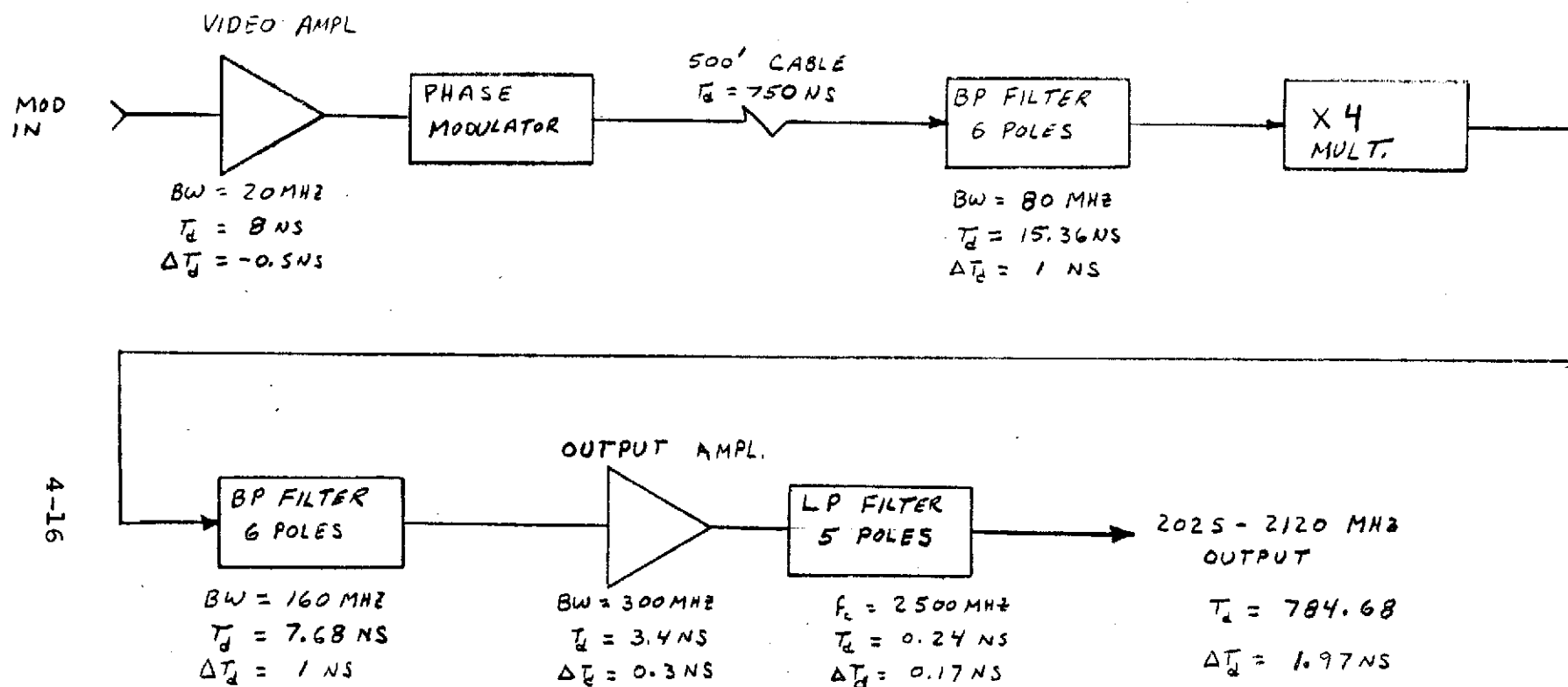
The differential time delays, Δt_d , given in Figure 4.3.1 are for a 5 MHz modulating frequency and in the case of the filters are for frequencies at the edge of the transmit band which is the worst case. The value of delay given for each stage is for low modulating frequencies for the video circuits and for mid-band operation in the case of the filters.

The total delay assuming 500 feet of RG-217 cable is 785 nanoseconds and the differential time delay is about 2 nanoseconds.

It should be noted that the video bandwidth of the modulator must be considerably larger than the 5 MHz specified in paragraph 4.3.1 in order to meet the differential delay specification.

The major source of long-term delay variation in the system is the cable between the Operations Control Building and the antenna-mounted equipment. This cable has a temperature coefficient of delay of about 200 ppm/°C.

The only significant sources of delay in the Frequency Translator are the coaxial cable between the Exciter output amplifier which may be up to 200 feet long and the output bandpass filter. The cable delay is about 300 nanoseconds. Differential filter delay is less than 1 nanosecond.



EXCITER TIME DELAY DISTRIBUTION

FIGURE 4.3.1

4.4 Exciter VCXO Offset Decay

When the exciter mode control switch is thrown from Search to Lock, the VCXO will have a frequency offset caused by the VCXO control voltage which is the sum of manual tuning plus sweep voltages. Let this voltage be called E offset.

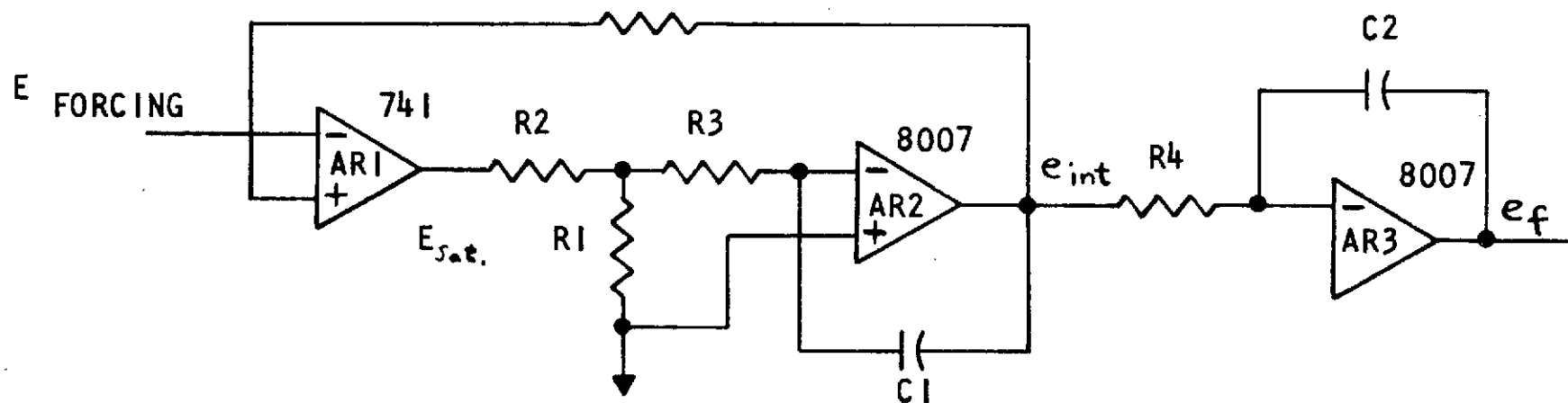
A voltage called E forcing, or E_{F1} , is generated to cause the VCXO to gradually return to center frequency where it can lock to the station standard. The rate of return is switched to be different for different exciter tracking loop bandwidths.

Figure 4.4.1 shows a typical configuration for one decay rate. Figure 4.4.2 shows the voltage waveforms as decay progresses.

E_{F1} is applied to AR1 at $t = 0$, where it is compared with the output of AR2. AR1 will saturate and a portion of this saturation voltage will be integrated by AR2, C_1 and R_3 into a ramp. When the output of AR2, called $e_{int.}$, is equal to E_{F1} at the input to AR1, the output of AR2 will stop integrating and will hold the value E_{F1} . This occurs at T_1 of Figure 4.4.2.

The ramp of $e_{int.}$ is again integrated by AR3, R_4 , and C_2 . This part of the curve is a parabola, accelerating toward zero voltage. At time T_1 , the output of AR3 (called e_f) becomes a straight line sloping toward zero.

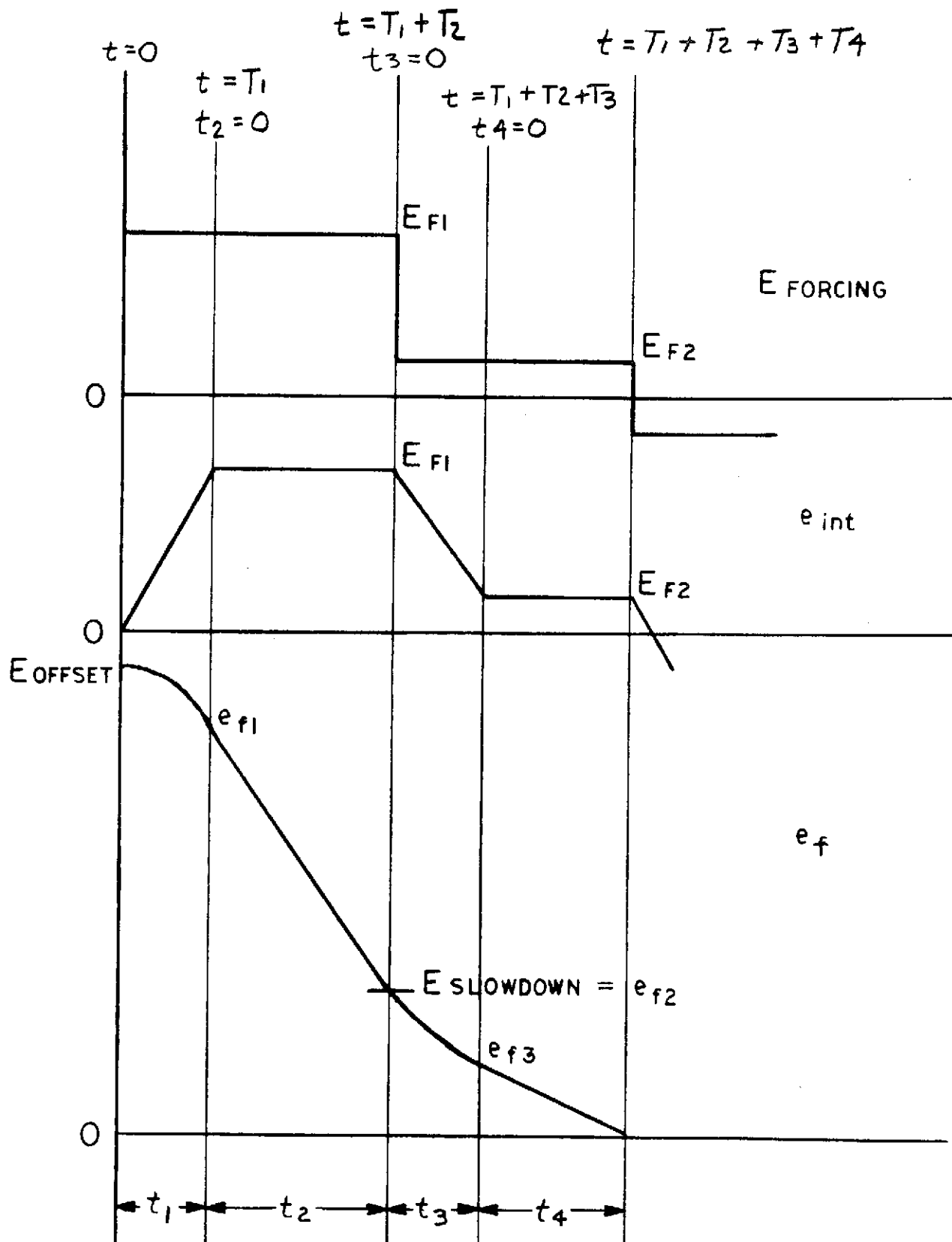
As the frequency of the VCXO approaches the station standard, the beatnote is used to cause slowdown. The input E_{F1} falls to E_{F2} , about one-tenth as large. This occurs at T_2 .



ASSUME 741
 OUTPUT = $\pm 13V$
 = $\pm E_{sat}$

DECAY VOLTAGE
 INTEGRATOR DIAGRAM

FIG. 4.4.1



INTEGRATOR WAVEFORMS
 FIG. 4.4.2

Again AR1 will compare the new input with e_{int} and saturate in the proper direction. The circuits of AR2 will integrate a ramp to the new voltage level and stop at time T_3 and at E_{F2} volts.

AR3 again makes a parabolic transition from T_2 to T_3 . It then assumes a more gradual straight line toward zero volts. If the rate is slow enough lock will occur in the region of zero volts. If lock fails to occur, and the VCXO overshoots, the forcing function E_{F2} will reverse polarity, bringing the VCXO repeatedly back to the correct frequency, even though this may not occur exactly at zero volts.

Computed Constants for Fig. 4.4.2

	Wide		Medium		Narrow	
Starting frequency, Δf , at S-Band	150	kHz	150	kHz	15	kHz
$E_{\text{offset}} = \frac{\Delta f}{40 \text{ kHz/V}}$	3.75		3.75		.375	volts
T_1	.00784		.029		.29	sec
$e_{F1} = E_{\text{offset}} - \frac{1}{2} \times 5 \frac{T_1^2}{R_3 C_1 R_4 C_2}$	3.74		3.75		.373	volts
f_{slowdown} , referred to S-Band	5400		1256		636	Hz
$E_{\text{slowdown}} = \frac{f_{\text{slowdown}}}{40 \text{ kHz/V}}$.135		.0314		.0159	volts
T_2	1.208		18		25.4	sec
T_3	.00711		.0264		.264	sec
e_{f3}	.1236		.0283		.01686	volts
T_4	.455		1.51		13.2	sec
T_{total}	1.78		19.6		39.2	sec

5.0 SYSTEM TESTING

5.1 General

The acceptance testing for the exciters will be performed according to the Design Verification Tests (DVT) and the Performance Acceptance Tests (PAT) defined in item 4 of the contract schedule. Briefly, the purpose of the DVT is to demonstrate that all of the performance requirements for the equipment have been achieved in the completed design.

The purpose of the PAT is to demonstrate that the production units perform to the same level as the design verification units.

The DVT is necessarily a more rigorous and time consuming task than the PAT task. Parameters which are included in DVT, but omitted from PAT will consist of: those parameters which, once proven acceptable, are unlikely to vary significantly in the production units; or, can be verified by valid but indirect measurements. Those measurements which are to be included in the PAT consist of simplified, or sampled, portions of the DVT procedure in sufficient detail to establish correlation with the DVT results.

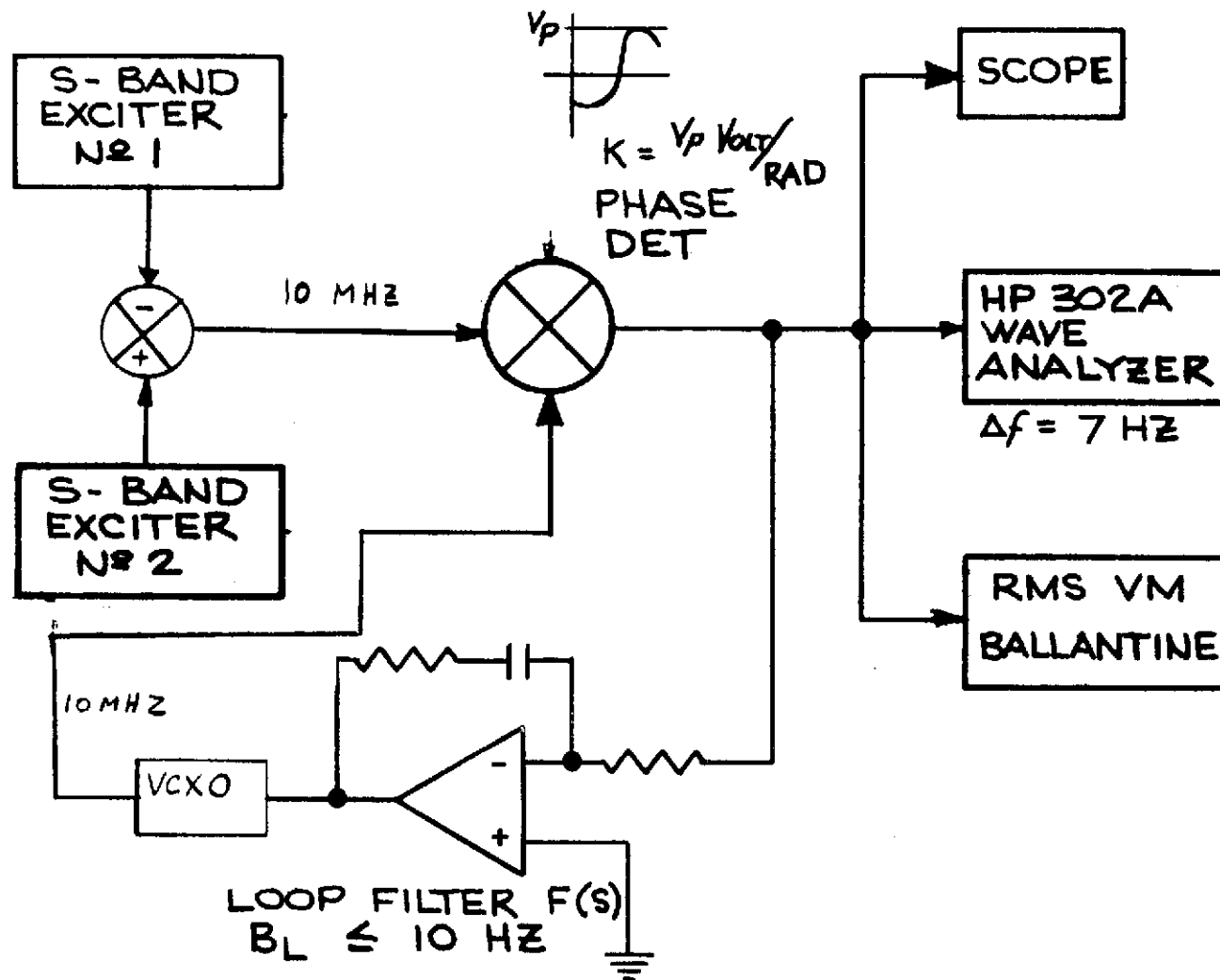
5.2 S-Band Exciter Acceptance Tests

The following methods are suggested as examples of DVT and PAT procedures for the specified parameters.

a) Phase noise and phase jitter - The phase noise of the S-Band Exciters will be measured using a test set-up similar to that shown in Figure 5.2.1. In the set-up, two S-Band Exciters, set for a 10 MHz frequency difference, are mixed and the resulting 10 MHz signal is locked to a stable VCXO in a narrow bandwidth phase locked loop. The output of the phase detector is measured to determine the phase noise. Equal contributions of phase noise are ascribed to each exciter. Calibration of each exciter's noise power can be made by comparing each against a third unit. Phase noise and jitter will be measured as both DVT and PAT.

b) Time Delay - The time delay requirements for the exciter are easier to design than to measure. It is suggested that differential time delay measurements be performed on each of the subassemblies in the modulation signal path. Using standard techniques, such as a vector voltmeter to determine the phase slope versus frequency, the differential delay of the major components in the modulation signal path can be determined. By numerical methods, then, the total differential delay of the system can be determined.

The delay stability of the system, as a function of time, is best determined when all subsystems are integrated on the site, with the final configuration of interconnecting cables in place. Measurements can be made before shipment, however, to determine the overall stability of the system,



PHASE NOISE TEST SET UP

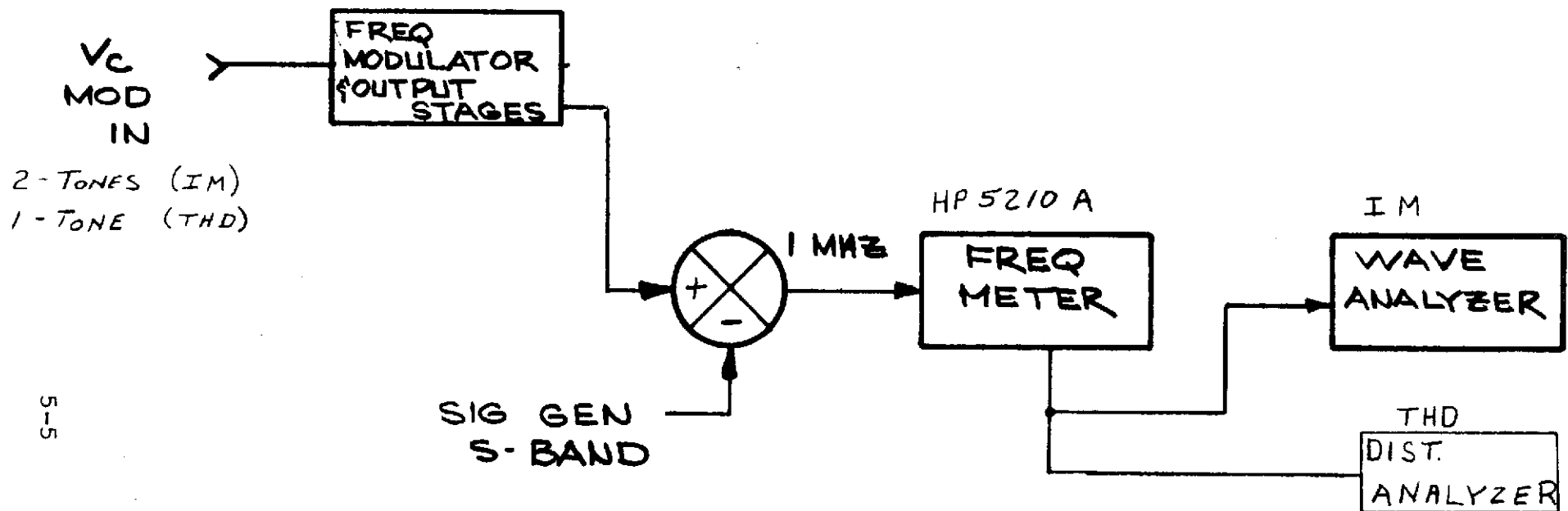
FIGURE 5.2.1

baseband to baseband, through the Verification Receiver.

It is intended that the time delay measurements be performed as design verification tests.

c) Spurious Response - The measurement of spurious output signals from the exciter can be performed easily using commercially available spectrum analyzers, with the exception of the 2200-2300 MHz band. In this band the spurious specification of -177 dB can not be measured with commercial equipment. For this requirement an indirect measurement is an accepted method of determining spurious levels. That is, by knowledge of spurious levels in the early stages of the exciter, and by measurement of filter attenuation characteristics in the exciter final stages, the overall spurious levels can be determined.

d) Modulator Linearity - The FM and PM modulator third order IM and total harmonic distortion can be measured using the test set-ups of Figure 5.2.2 and 5.2.3. For the FM test both IM and THD can be measured directly using the HP5210A linear frequency discriminator. However, for PM the discriminator output must be integrated to determine the THD. If sine wave modulation is used and the frequency separation is small the third order IM measurement can be made directly. These tests will be both DVT and PAT.

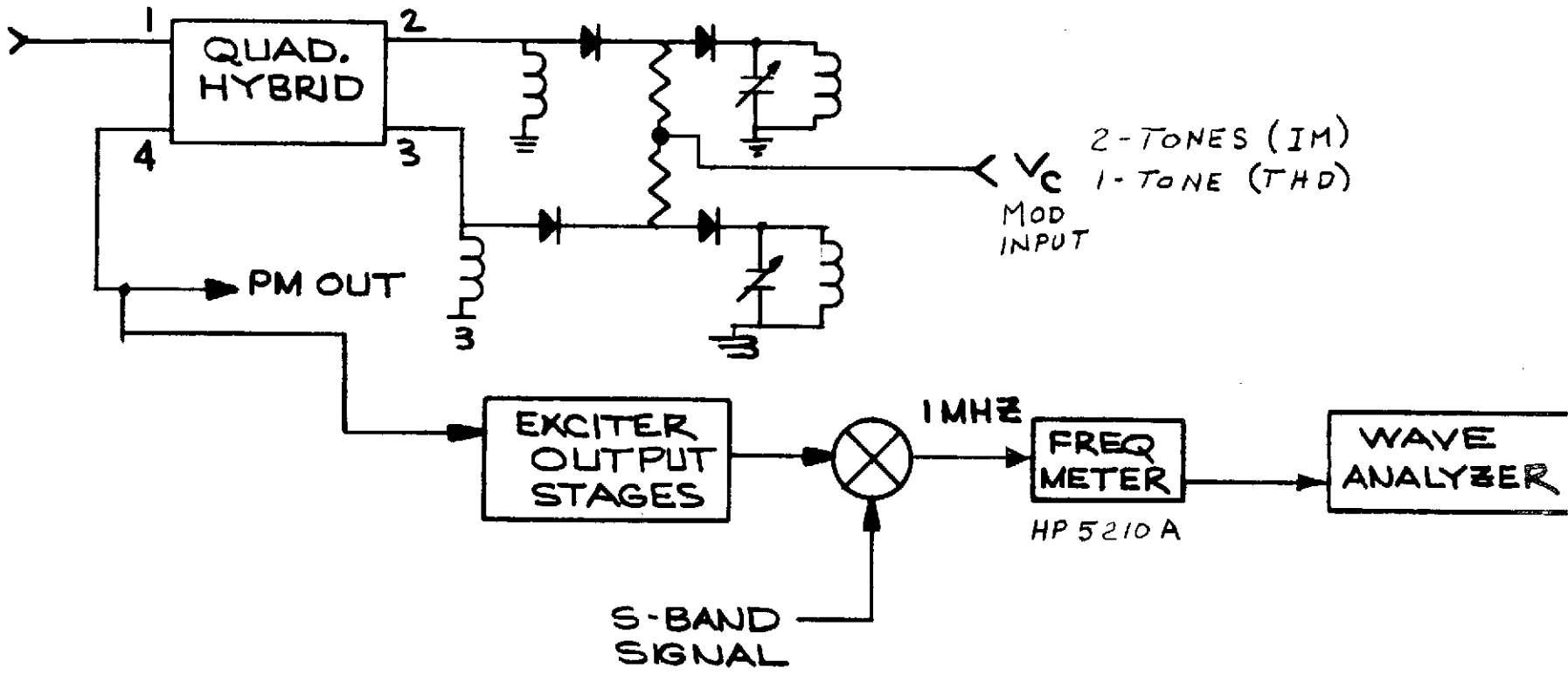


FM DISTORTION TEST SET-UP

FIGURE 5.2.2

506.25 -
530
MHz
INPUT

PHASE MODULATOR



5-6

PM DISTORTION TEST SET-UP

FIGURE 5.6.3

APPENDIX I

5 MHZ FREQUENCY STANDARD

SPECIFICATION

APPLICATION			REVISIONS		
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
0482-1000	MFR		RELEASED FOR PRODUCTION	28 NOV 73	TJ

1.0 SCOPE: THIS SPECIFICATION COVERS THE DETAIL REQUIREMENTS FOR A 5 MHZ FREQUENCY STANDARD.

2.0 APPLICABLE DOCUMENTS: NONE

3.0 DETAIL REQUIREMENTS:

3.1 FREQUENCY: 5 MHZ, SETTABLE TO ± 1 PART IN 10^9 RESOLUTION WITH MANUAL FREQUENCY ADJUSTMENT.

3.1.1 DRIFT WITH TEMPERATURE: ± 1 PART IN 10^8 MAXIMUM OVER AMBIENT TEMPERATURE RANGE OF 0°C TO 55°C.

3.1.2 SHORT TERM STABILITY: LESS THAN ± 3 PARTS IN 10^{11} PER SECOND RMS. (MEASURED AT CONSTANT AMBIENT.)

3.1.3 DRIFT WITH TIME: ± 5 PARTS IN 10^9 PER DAY MAXIMUM AFTER 24 HOURS MINIMUM WARMUP. (MEASURED AT CONSTANT AMBIENT.)


3.1.4 FREQUENCY ADJUSTMENT RANGE: SHALL BE ENOUGH TO COVER A 5 YEAR AGING PERIOD.

4.0 ELECTRICAL REQUIREMENTS:

4.1 INPUT SUPPLY:

4.1.1 OSCILLATOR: +15 ± 1 VDC AT 50 MA MAXIMUM.

SPECIFICATION CONTROL DRAWING

ALL DIM. IN INCHES TOLERANCES FRACTIONS $\pm 1/64$ ANGLES $\pm 1^\circ$ DEC XX $\pm .02$ XXX $\pm .005$		DR <i>R. Pate</i> 21-NOV-73	 RF COMMUNICATIONS INC. ROCHESTER, NEW YORK, USA		
MFG SPEC:		CHK <i>VEL</i> 21-NOV-73			
MATL:		ENGR <i>R. King</i> 11/27/73	TITLE FREQUENCY STANDARD		
FIN.:		APPD <i>TJ</i> 11/27/73			
		CONTR NO. NAS5-20473	REL DATE 28 NOV 73		
		DSGN ACTIVITY APPROVAL		SIZE A	CODE IDENT NO. 14304
		APPROVED		DRAWING NO. 0482-3015	REV
				SCALE	WEIGHT
				SHEET 1 OF 3	

4.1.2 OVEN: (PROPORTIONAL CONTROLLED) +28 \pm 2 VDC AT 5 WATTS
AVERAGE AFTER WARMUP.

4.2 OUTPUT WAVEFORM:

4.2.1 HARMONICS: -30 db MINIMUM INTO 50 OHM LOAD.

4.2.2 SIGNAL-TO-AM NOISE RATIO: -80 db MINIMUM.

4.2.3 SINEWAVE: 1 V RMS MINIMUM INTO 50 OHM.

4.2.4 SHORTING OF OUTPUT LEADS SHALL CAUSE NO INTERNAL
DAMAGE.

4.2.5 SIGNAL-TO-PHASE NOISE RATIO: -85 db MINIMUM IN A
30 KHz BAND CENTERED AT 5 MHz AND EXCLUDING A 1 Hz BAND
CENTERED AT 5 MHz.

4.2.6 SPECTRAL PURITY - SSB S/N (db):

4.2.6.1 110 db, 2 Hz REMOVED FROM CARRIER.

4.2.6.2 120 db, 10 Hz REMOVED FROM CARRIER.

4.2.6.3 125 db, 100 Hz REMOVED FROM CARRIER.

4.2.6.4 134 db, 500 Hz TO 5 KHz REMOVED FROM CARRIER.

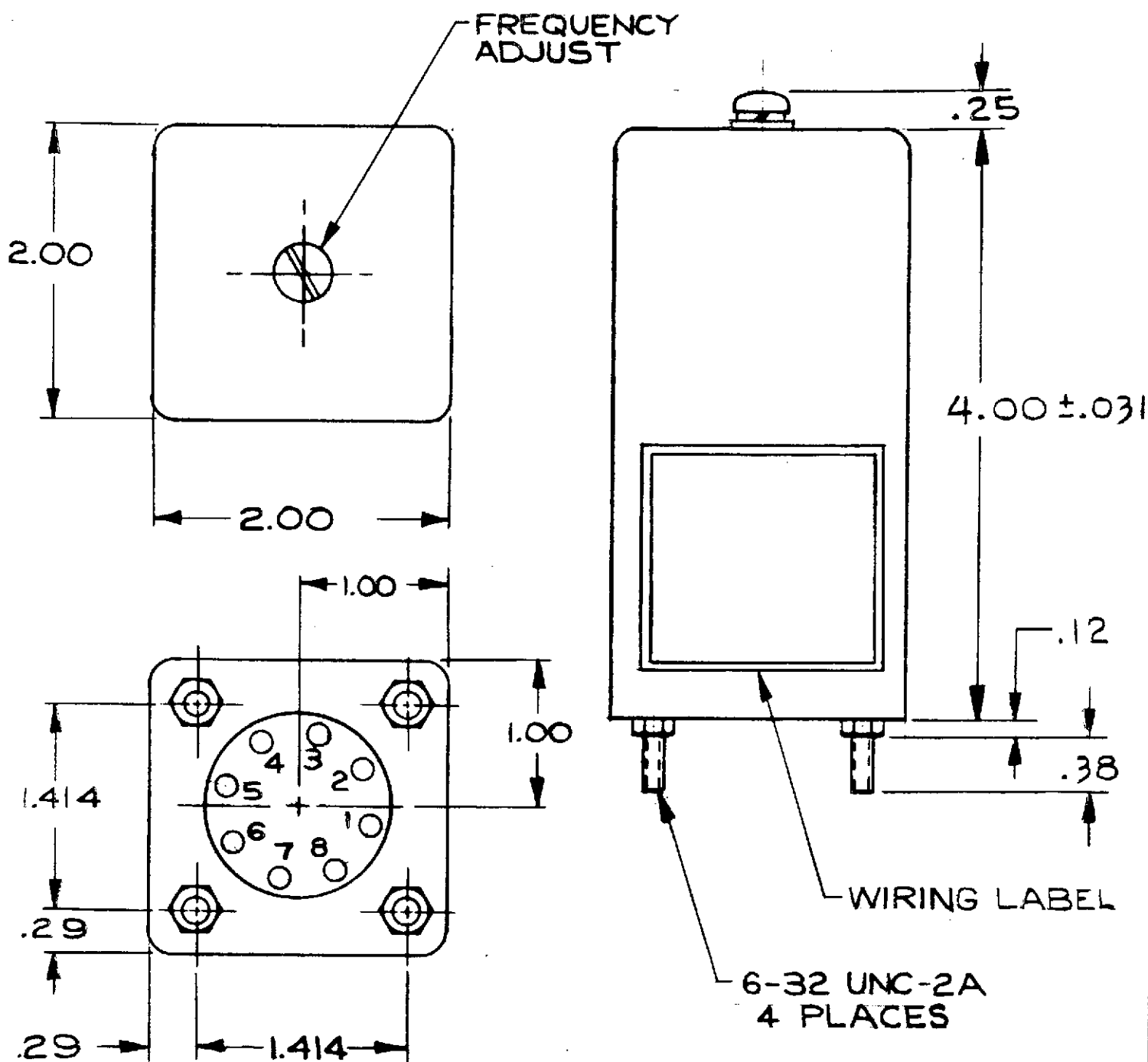
5.0 MECHANICAL: SEE FIGURE 1.

5.1 FREQUENCY STANDARD PIN CONNECTIONS:

- 1 28V RETURN (OVEN)
- 2 +15VDC (OSCILLATOR)
- 3 +28VDC (OVEN)
- 4 N.C.
- 5 N.C.
- 6 5MHz OUT
- 7 15V RETURN
- 8 SIGNAL GROUND

SIZE	CODE IDENT NO.		
A	14304	0482-3015	
SCALE	—	—	SHEET 2 OF 3

↑



SIZE	CODE IDENT NO.	0482-3015	
A	14304		
SCALE	—	—	SHEET 3 OF 3

APPENDIX II

AN MTBF CALCULATION AND

PERCENT OPERABILITY PREDICTION

Appendix II is a mean-time-between-failure (MTBF) and a mean-time-to-repair (MTTR) prediction for the S-Band exciter equipment. These predictions are based on preliminary parts estimates and were performed in accordance with guidelines established in MIL-HDBK-217A and MIL-HDBK-472 handbooks.

EXCITER
MTBF

	Stress Ratio/ TN	Ground Failure Rate	Qty.	Total Failure Rate
CAPACITOR, MICA DIP	.3	.0010	137	.137
CAPACITOR, MET FILM	.5	.3770	4	1.508
CAPACITOR, VAR PISTON	.1	.0210	10	.210
CAPACITOR, VAR AIR	.1	.0060	26	.156
CAPACITOR, CER	.5	.0036	1027	3.697
CAPACITOR, ELECTROLYTIC ALUM.	.7	.0420	2	.084
CAPACITOR, SOLID TANTALUM	.6	.0820	86	7.052
RESISTOR, CARBON	.4	.0210	1495	32.395
RESISTOR, FILM	.1	.0750	13	.975
RESISTOR, VAR COMP	.6	1.0000	34	34.000
DIODE, SI	.5	.6150	143	87.945
DIODE, SI RECT.	.7	2.4600	2	4.920
DIODE, ZENER	.3	.7700	34	26.180
TRANSISTOR, SI PNP POWER	.5	2.5000	6	15.000
TRANSISTOR, SI NPN	.5	.6150	280	172.200
TRANSISTOR, SI NPN POWER	.7	.8200	1	.820
TRANSFORMER		.3300	202	66.660
INDUCTOR, FIXED		.3300	206	67.98
CIRCUIT BREAKER		1.0000	1	1.000
INTEGRATED CIRCUIT, ANALOG	.5	.8000	60	48.000
INTEGRATED CIRCUIT, DIGITAL	.5	.4000	98	39.200
INTEGRATED CIRCUIT, HYBRID	.5	.8000	14	11.200
SWITCH	.5	1.0000	30	30.000
RELAY	.5	1.0000	2	2.000

EXCITER
MTBF

	Stress Ratio/ TN	Ground Failure Rate	Qty.	Total Failure Rate
CONNECTOR, MULTIPIN	.5	.3000	36	10.800
CONNECTOR, COAX	.2	1.0000	78	78.000
MIXER	.2	4.8000	20	96.000
FILTER	.7	1.0000	27	27.000
METER, PANEL	.2	.5000	4	2.000
POWER SUPPLY	.7	25.0000	3	75.000
FREQ STANDARD	.5	5.0000	1	5.000
DISPLAY	.7	7.5000	4	30.000
LAMPS, INCANDESCENT	.7	1.0000	<u>113</u>	113.000
	Total Parts		<u>4199</u>	
F.R./million hrs. at 40°C				1089.119
MTBF in hours				918.173
F.R./million hrs. at 40°C (excluding lamps)				976.119
MTBF in hours (excluding lamps)				1024.465

ANTENNA ELECTRONICS
MTBF

	Stress Ratio/ TN	Ground Failure Rate	Qty.	Total Failure Rate
CAPACITOR, MICA DIP	.3	.0360	1	.036
CAPACITOR, VAR PISTON	.1	.0590	18	1.062
CAPACITOR, CER	.5	.0100	38	.380
CAPACITOR, ELECTROLYTIC ALUM.	.7	.0950	2	.190
CAPACITOR, SOLID TANTALUM	.6	.1500	12	1.800
RESISTOR, CARBON	.2	.036	21	.756
RESISTOR, POWER WW	.5	.300	4	1.200
RESISTOR, VAR COMP.	.1	1.000	1	1.000
DIODE, RECT.	.6	1.850	8	14.800
DIODE, ZENER	.3	.770	3	2.310
TRANSISTOR, SI NPN	.3	.383	1	.383
TRANSISTOR, SI NPN POWER	.7	1.830	10	18.300
TRANSFORMER		.330	1	.330
INDUCTOR, FIXED		.330	18	5.940
INTEGRATED CIRCUIT, ANALOG	.5	.800	5	4.000
INTEGRATED CIRCUIT, HYBRID	.5	.800	5	4.000
RELAY	.5	1.000	2	2.000
CONNECTOR, MULTIPIN	.5	.300	10	3.000
CONNECTOR, COAX	.2	1.000	11	11.000
FILTER	.5	1.000	<u>5</u>	5.000
	Total Parts		176	
F.R./million hrs. at 70°C				77.487
MTBF in hrs.				12905.391

TRANSLATOR
MTBF

	Stress Ratio/ TN	Ground Failure Rate	Qty.	Total Failure Rate
CAPACITOR, MICA DIP	.3	.0010	3	.003
CAPACITOR, CER	.5	.0062	10	.062
RESISTOR, CARBON	.2	.0210	12	.042
RESISTOR, VAR COMP	.1	1.0000	5	5.000
RESISTOR, FILM	.1	.0900	8	.720
DIODE	.5	.6150	2	1.230
DIODE, ZENER	.3	.7700	2	1.540
TRANSISTOR, SI NPN	.3	.3830	1	.383
INTEGRATED CIRCUIT, ANALOG	.5	.8000	6	4.800
CONNECTOR, MULTIPIN	.5	.3000	5	1.500
MIXER	.2	4.8000	1	4.800
FILTER	.5	1.0000	1	1.000
MOTOR		22.0000	<u>1</u>	22.000
	Total Parts		57	
F.R./million hrs. at 55°C				43.080
MTBF in hours				23212.600

MTTR

	Reliability	Maintenance Task Times (minutes)						
	Data Failure Rate/ 10 ⁶ hrs.	Prepare Time	Loc. Time	RM/RP Time	Align & Test Time	Secure Time	Repair Time	Maint. Minutes/ 10 ⁶ hrs.
EXCITER	976.119*	30	60	15	30	5	140	136656.66
ANT ELECTRONICS	77.487	45	30	25	20	10	130	10073.31
TRANSLATOR	43.080	60	20	25	20	30	155	6677.40
	1096.686	32.2	56.3	16.1	28.9	6.3	139.8	153407.37

QUANTITATIVE FACTORS - (hours)

MTBF	911.8	MTTR	2.3
MTBM	911.8	Unsched. Maint.	2556.8

AVAILABILITY FACTOR - .9974432

NOTES

- * Not including panel lamp failures
(panel lamp failures do not affect
system performance; a front panel
lamp test switch is provided).

APPENDIX III

CABLE ASSEMBLIES

OPERATIONS BUILDING TO ANTENNA

FREQUENCY TRANSLATOR TO ANTENNA CONTROL

FROM	TO	FUNCTION	NOTES
W120P1-A	W120P2-A	XMTR DRIVE OUTPUT	Shld.
B	B	XMTR ON/OFF	pair No. 1
C	C	SHL'D	
D	D	EXCITER SWEEP WAVEFORM	Shld.
E	E	EXCITER SWEEP RETURN	pair No. 2
F	F	SHL'D	
H	H	EXCITER SWEEP DETECTOR	Shld.
J	J	PA SWEEP DETECTOR	pair No. 3
K	K	SHL'D	
L	L	SWEEP ON/OFF SELECT	Shld.
M	M	SWEEP ON/OFF SELECT	pair No. 4
N	N	SHL'D	
P	P	TEST ON/TEST OFF SELECT	Shld.
R	R	VERIF RCVR INPUT SELECT	pair No. 5
S	S	SHL'D	
T	T	SERVO ATT CONTROL CW	Shld.
U	U	SERVO ATT CONTROL W	pair No. 6
V	V	SHL'D	
W	W	SERVO ATT CONTROL CCW	Shld.
X	X	SERVO TUNE INDICATOR	pair No. 7
Y	Y	SHL'D	
Z	Z	NOT USED	
AA	AA		
BB	BB		
CC	CC		
DD	DD		
EE	EE		
FF	FF		
HH	HH		
JJ	JJ		
KK	KK		
LL	LL		
MM	MM		
NN	NN		
PP	PP	NOT USED	
RR	RR	SWEEP ON/OFF INDICATOR	Shld.
SS	SS	COMMON GRD	pair No. 8
TT	TT	SHL'D	
UU	UU	NOT USED	
VV	VV		
WW	WW		
XX	XX	NOT USED	

CABLE ASSY W120/W220

7324-0120/0220

S-BAND EXCITER SYSTEM (OPERATIONS BUILDING TO ANTENNA)

[illegible]

CABLE ASSY W138/W238

7324-0138/0238

S-BAND EXCITER (FREQUENCY TRANSLATOR TO ANTENNA CONTROL)